TOE2/0" 96860660

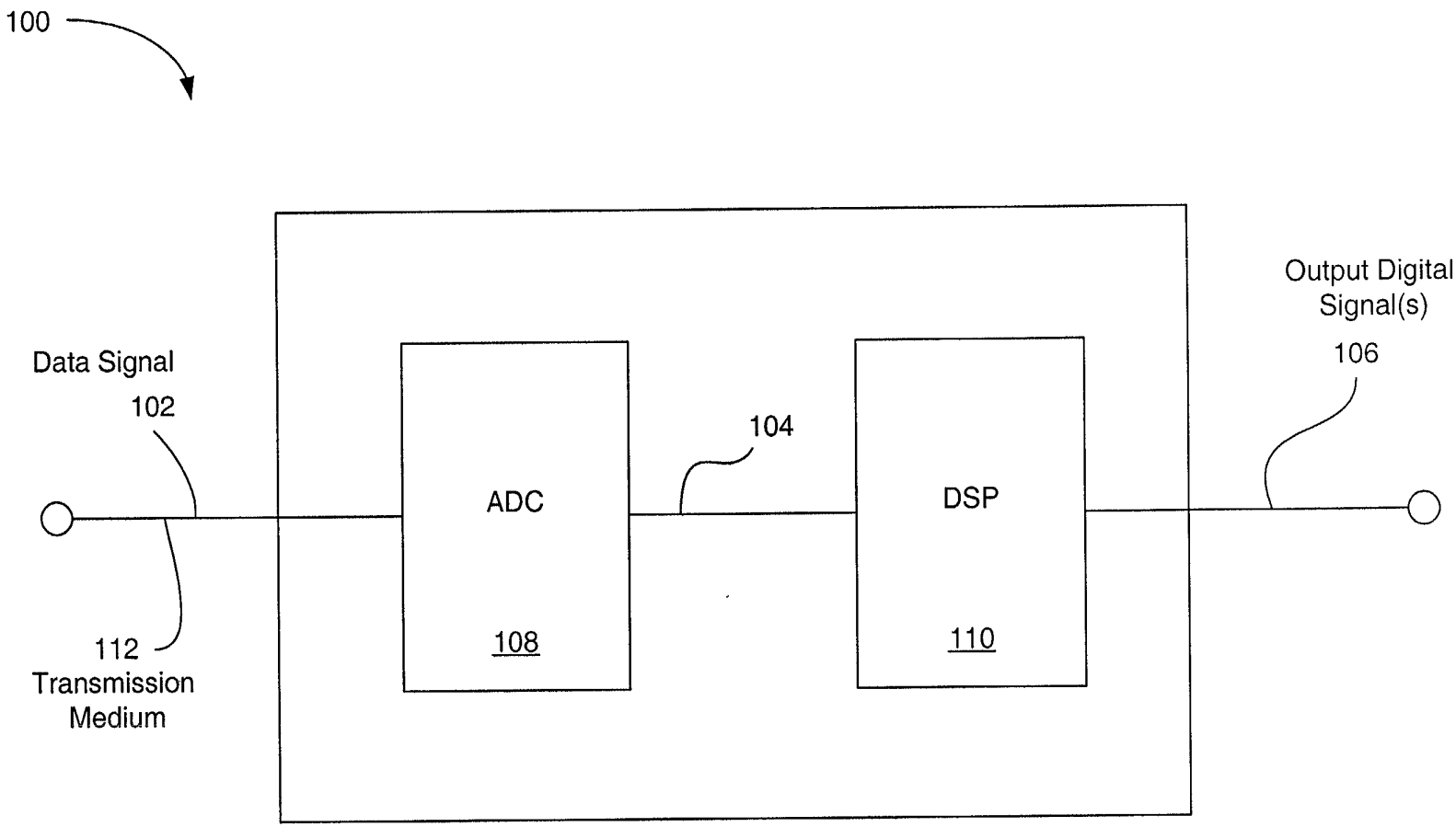


FIG. 1A

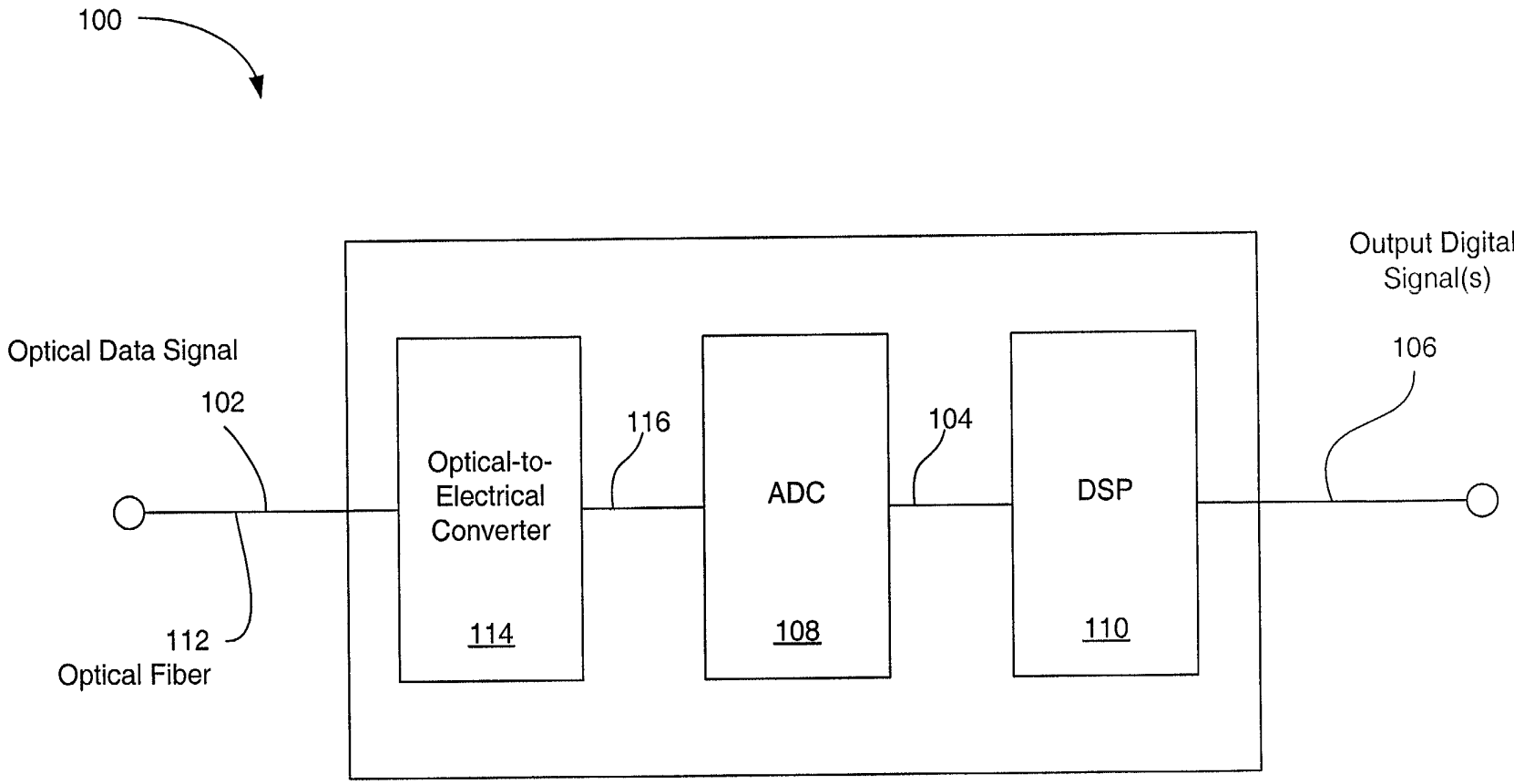

100
Optical Data Signal
102
112
Optical Fiber
Optical-to-Electrical Converter
114
116
ADC
108
104
DSP
110
106
Output Digital Signal(s)

FIG. 1B

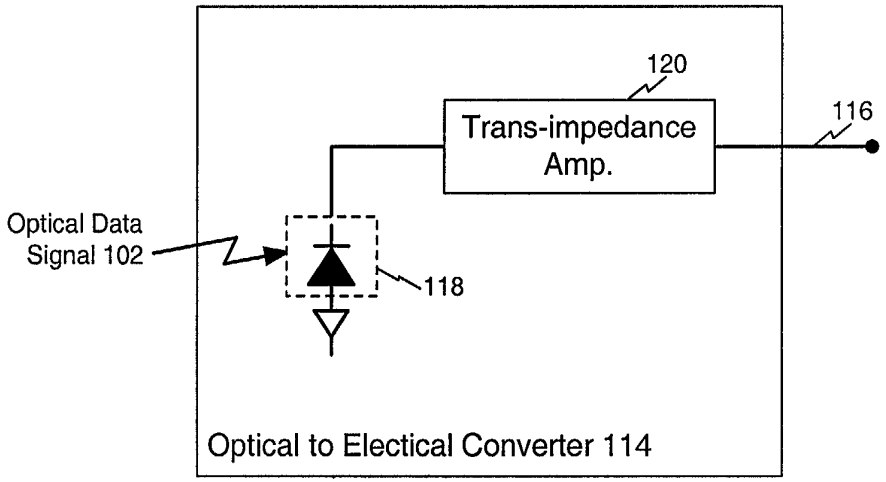

120
Trans-impedance Amp.
116
Optical Data Signal 102
118
Optical to Electical Converter 114

FIG. 1C

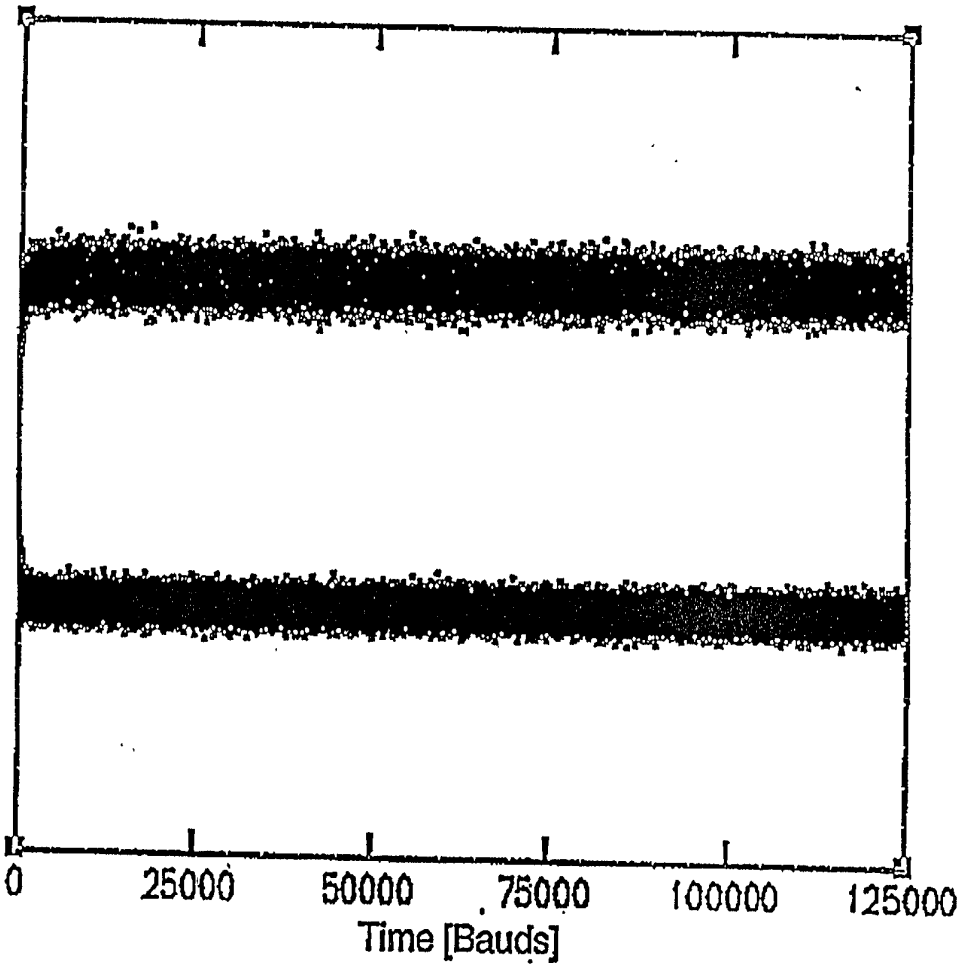


FIG. 2

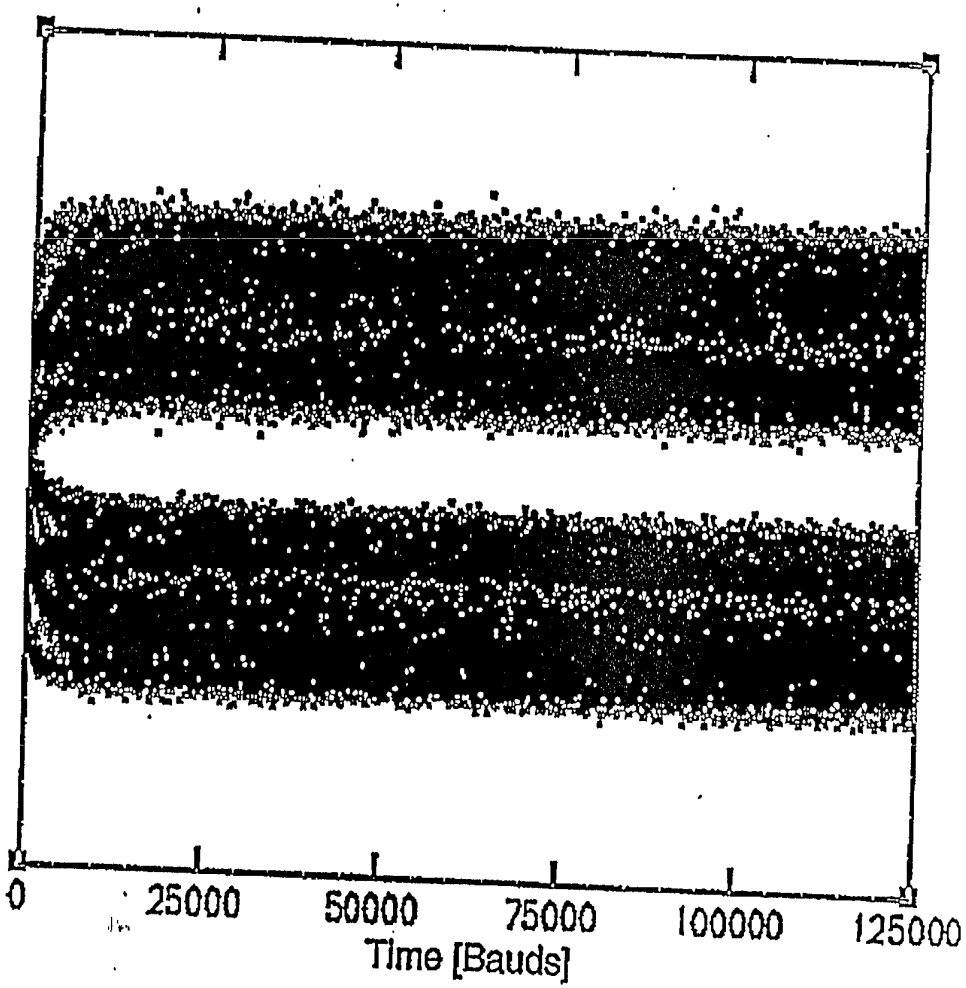


FIG. 3

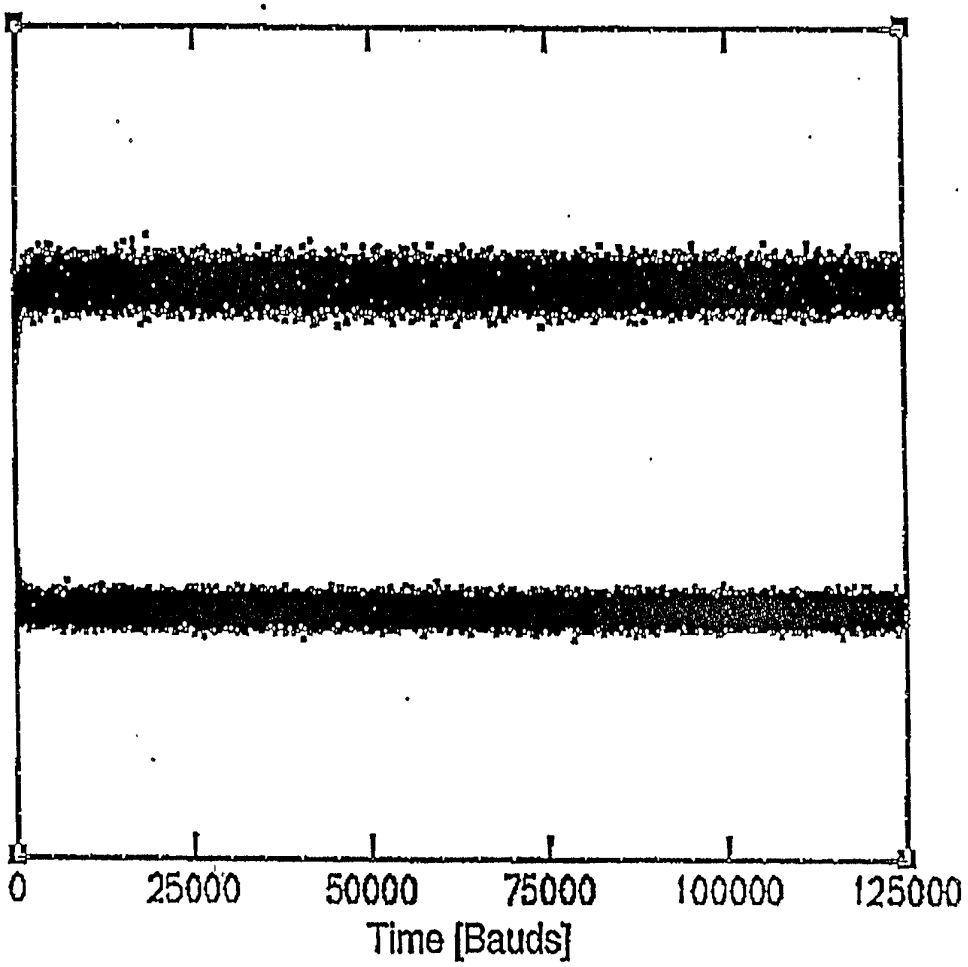


FIG. 4.

TDE2CD" 96860660

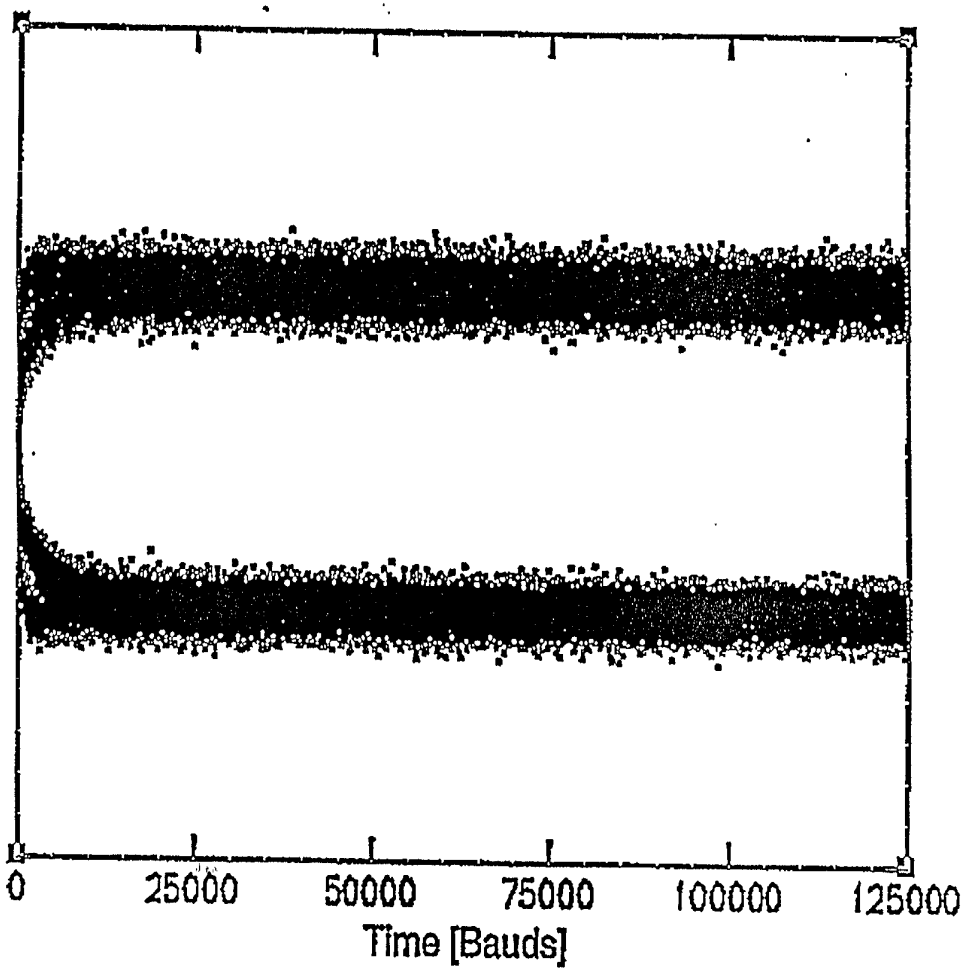


FIG. 5

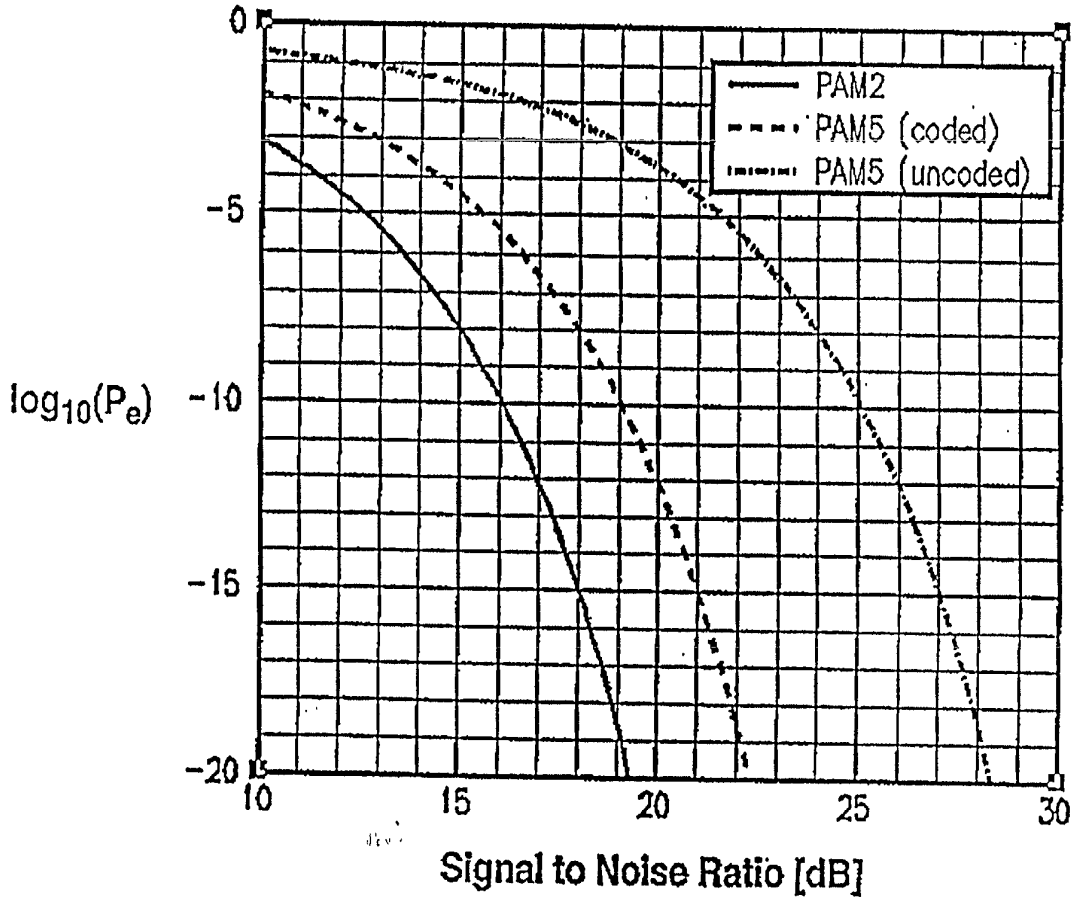

0
-5
-10
-15
-20
10
15
20
25
30
log10(Pe)
Signal to Noise Ratio [dB]
PAM2
PAM5 (coded)
PAM5 (uncoded)

FIG 6

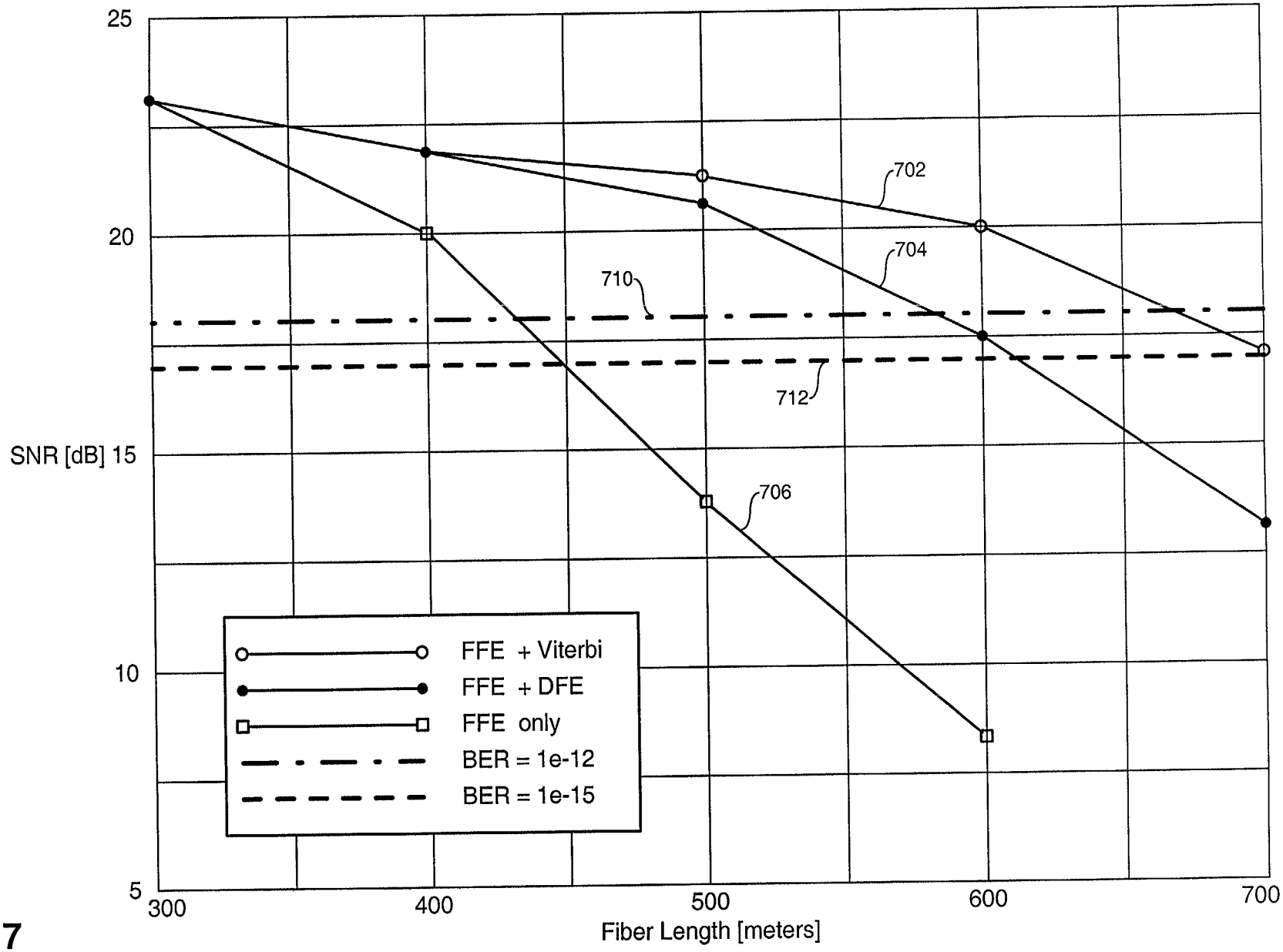


FIG. 7

SNR vs. Fiber Length for FFE, DFE and Viterbi Equalizer

0103-04.vsd/4

TOSZ20" 96860660

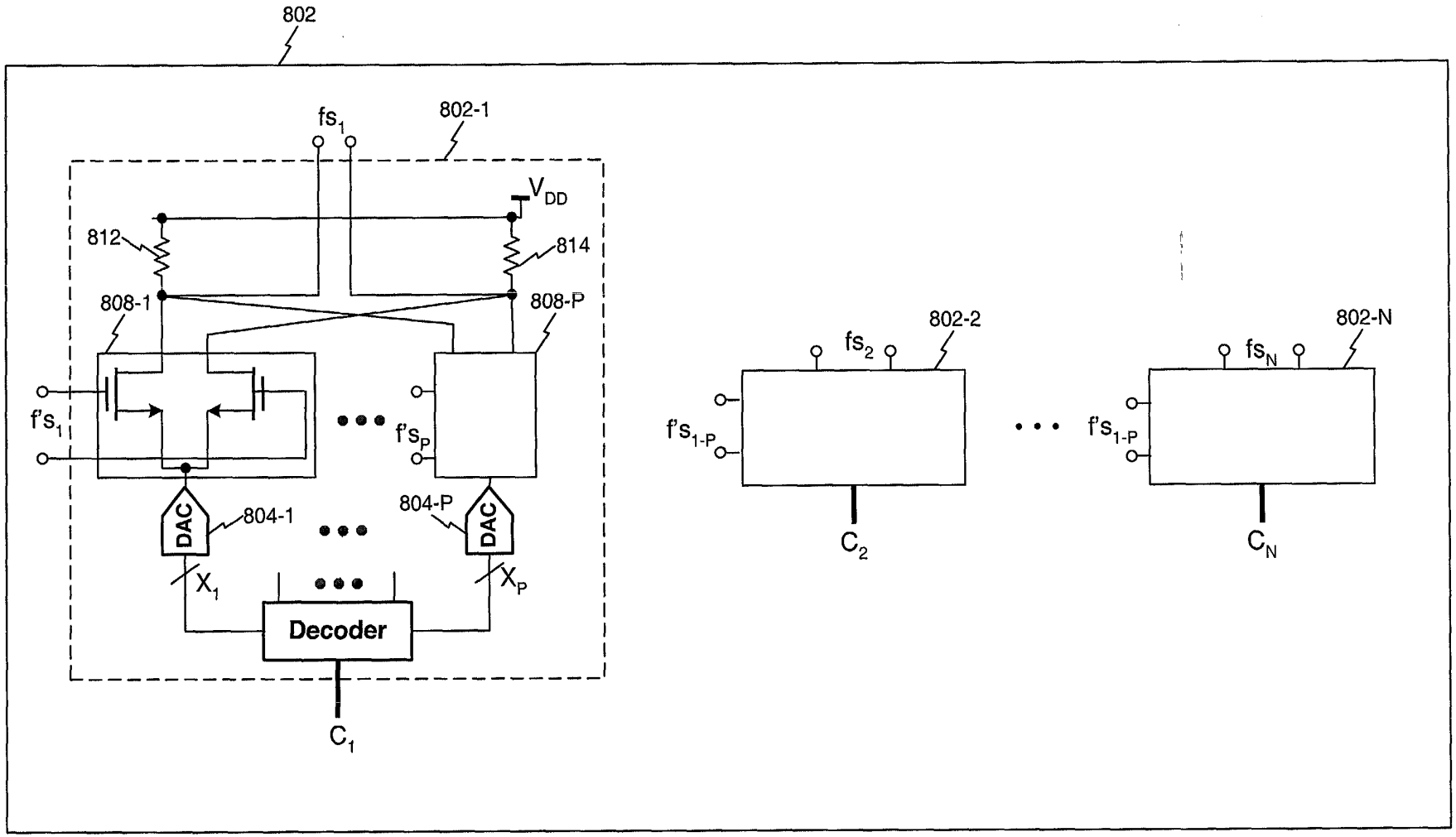


FIG. 8

TOE2.0" 96860660

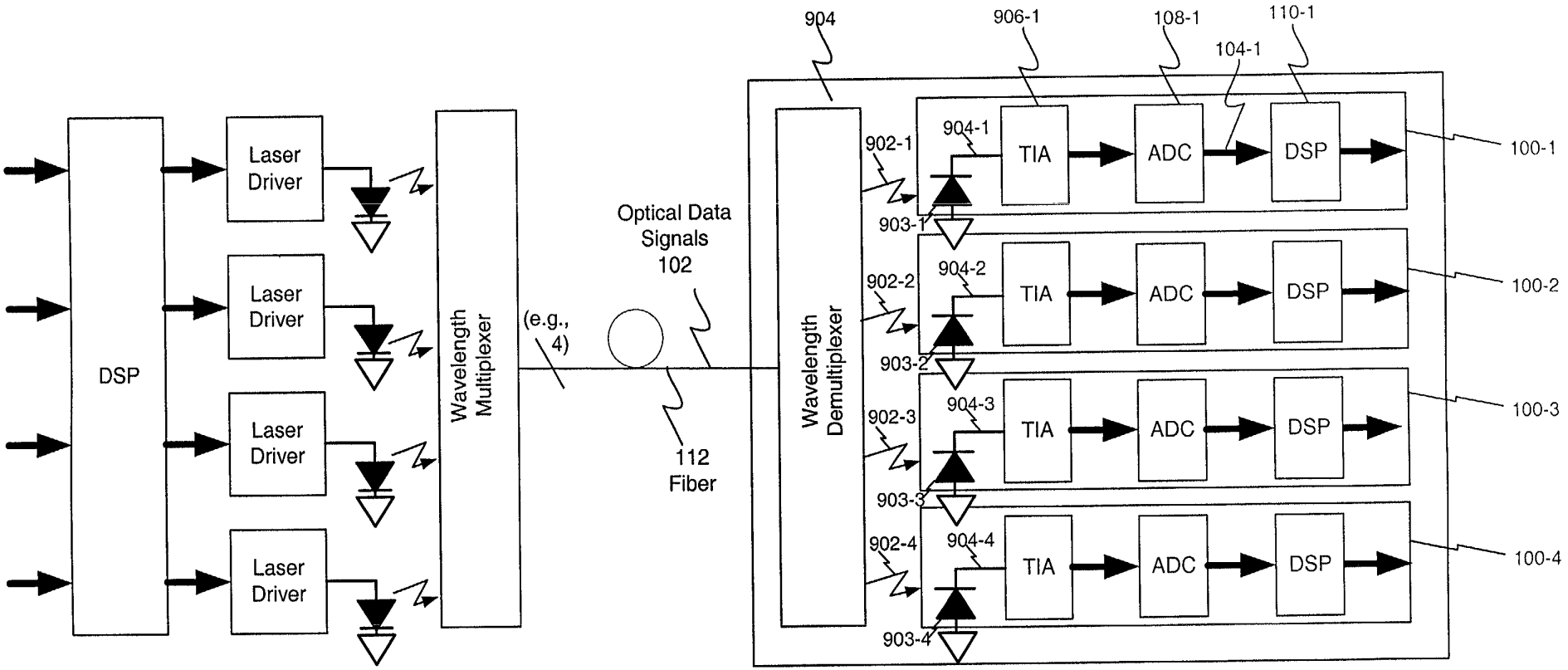


FIG. 9

0103-04.vsd/6

TOS2.0 96860660

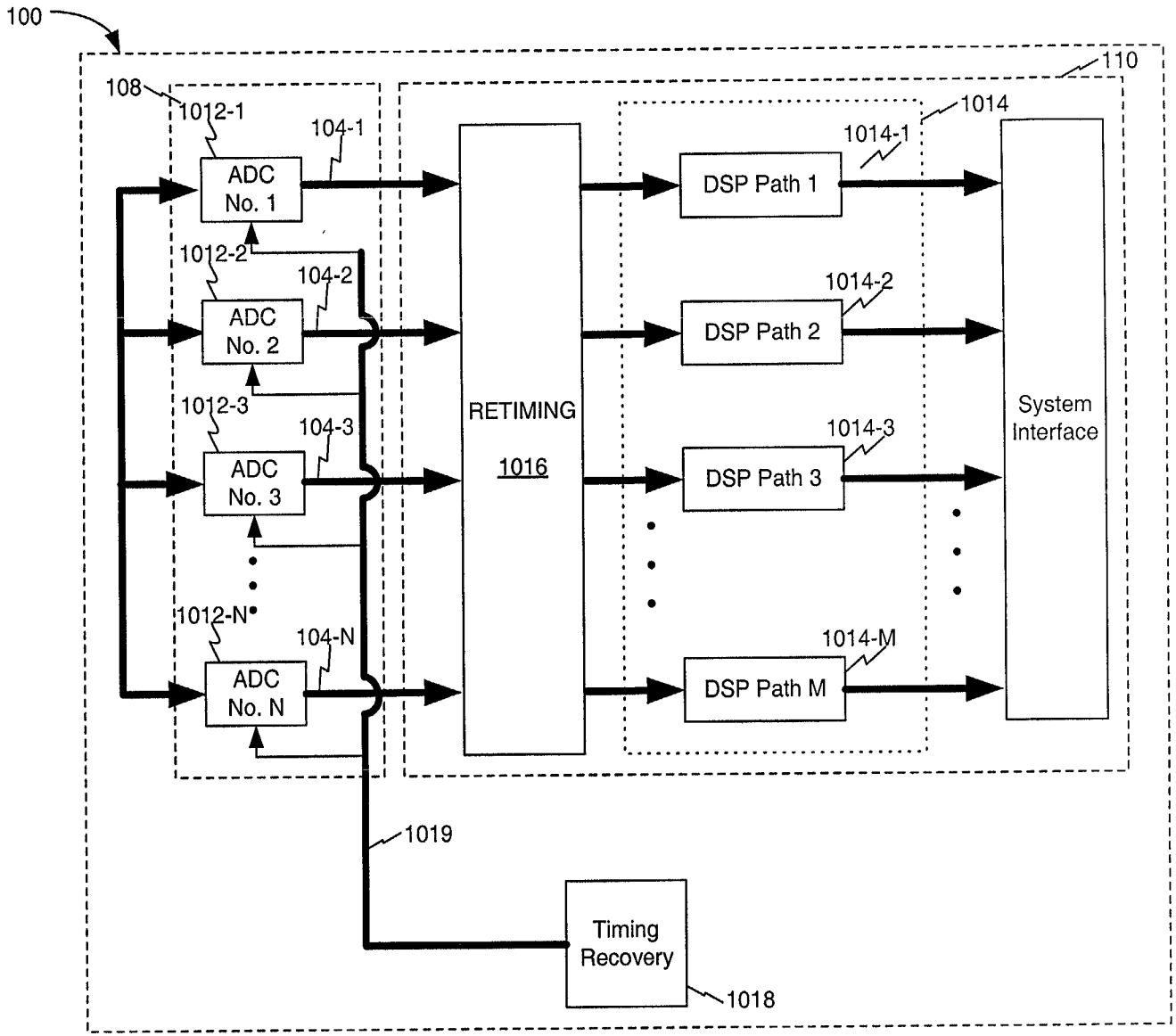


FIG. 10A

TOE220* 96860660

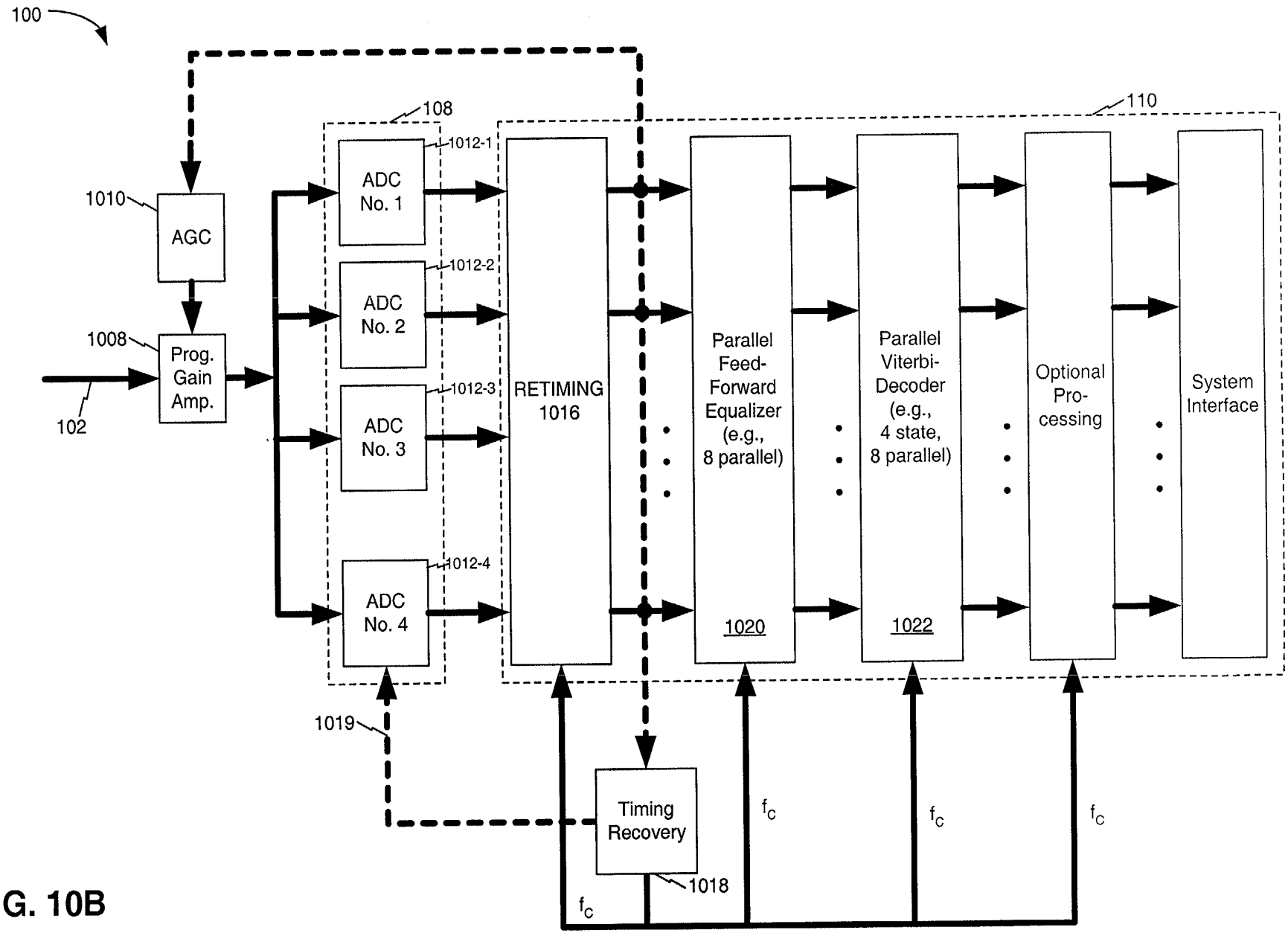


FIG. 10B

0103-04.vsd/8

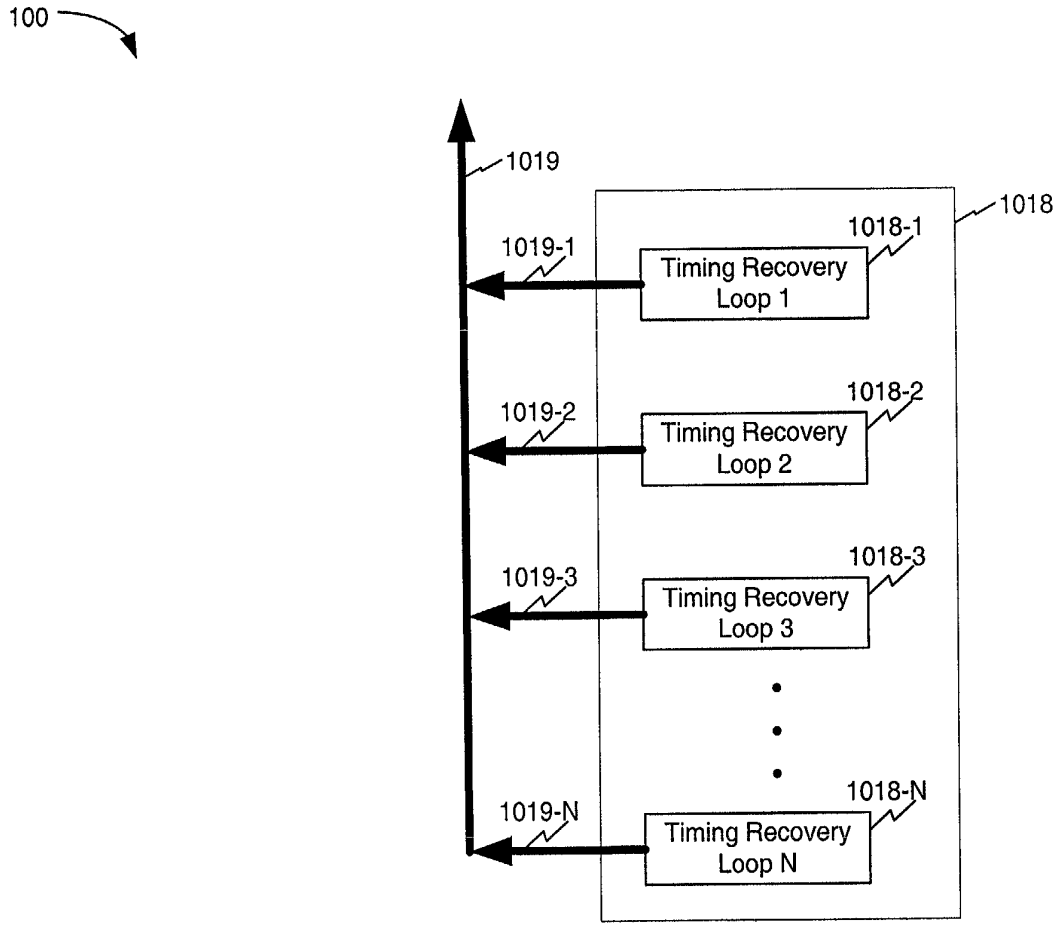

100
1019
1018
1018-1
1019-1
Timing Recovery Loop 1
1018-2
1019-2
Timing Recovery Loop 2
1018-3
1019-3
Timing Recovery Loop 3
1018-N
1019-N
Timing Recovery Loop N

FIG. 10C

TOE240 96860660

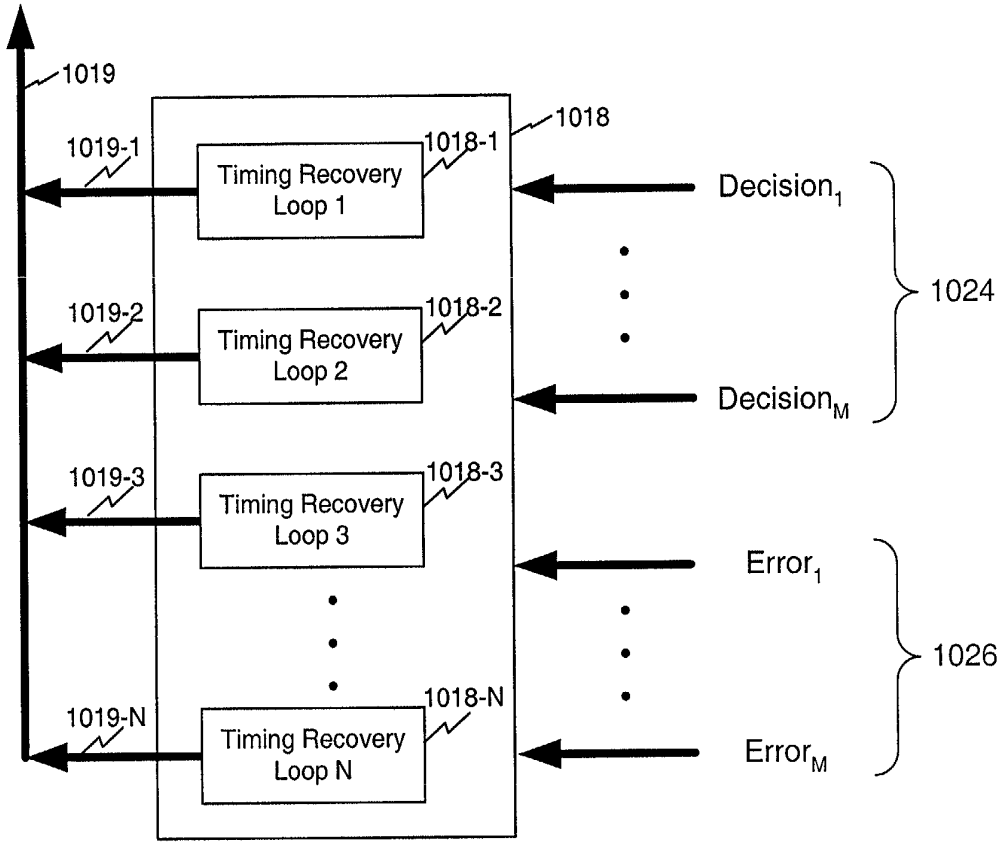


FIG. 10D

TOC20" 96860660

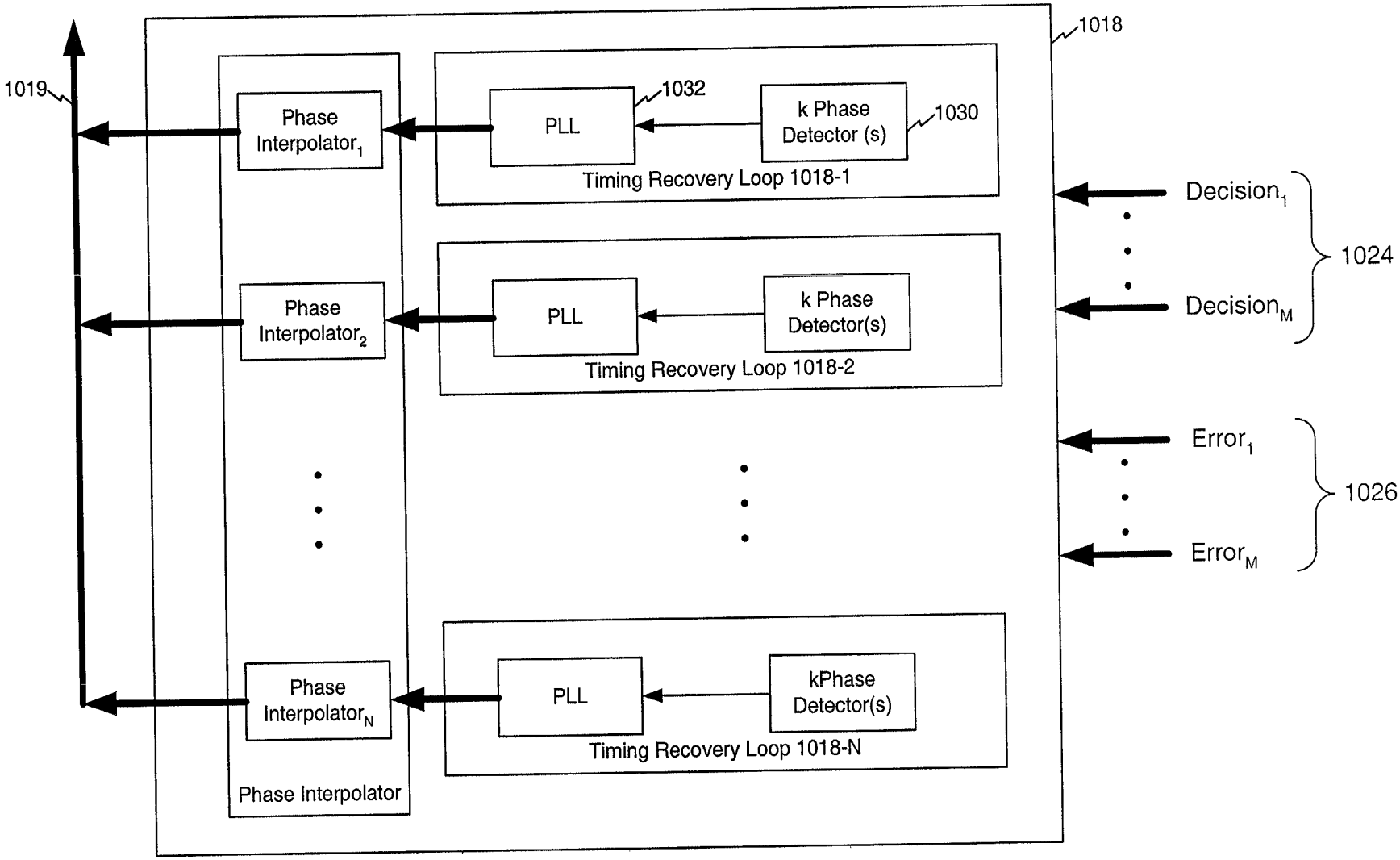


FIG. 10E

TOE220" 96860660

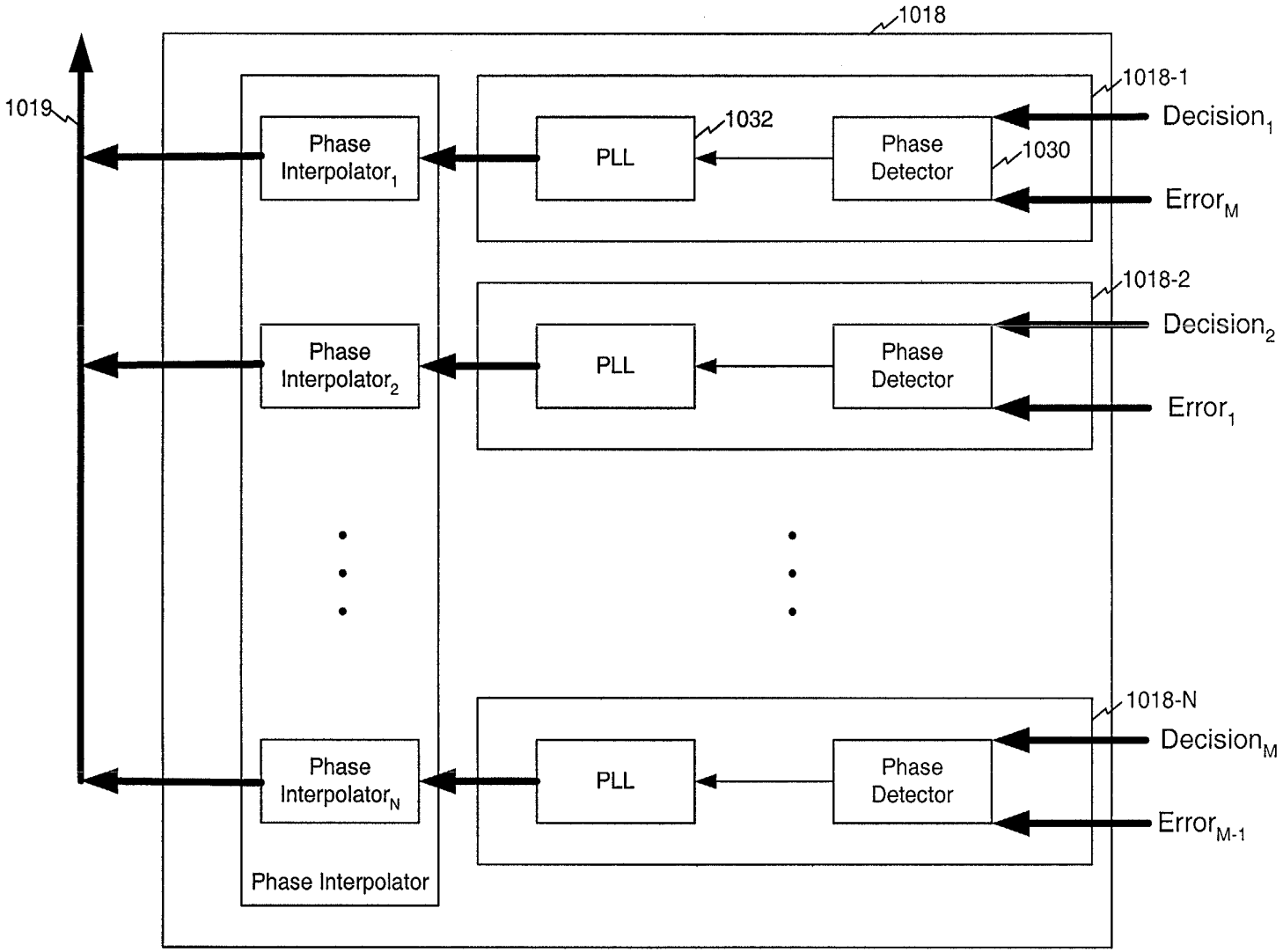


FIG. 10F

0103-04.vsd/12

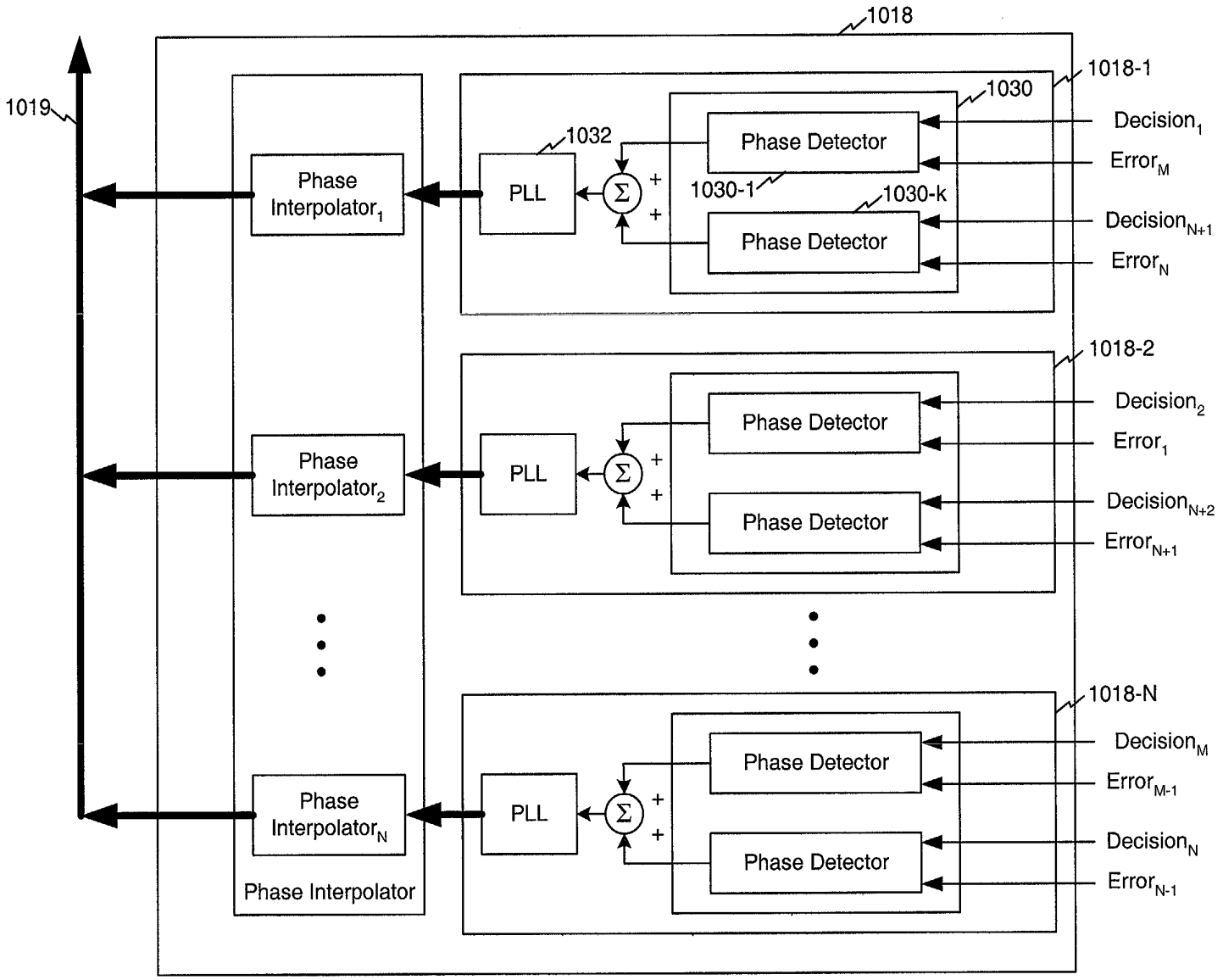

1018
1019
1018-1
1030
1032
Phase Detector
PLL
Phase Interpolator1
1030-1
1030-k
Phase Detector
Decision1
ErrorM
DecisionN+1
ErrorN
1018-2
Phase Interpolator2
Decision2
Error1
DecisionN+2
ErrorN+1
1018-N
Phase InterpolatorN
DecisionM
ErrorM-1
DecisionN
ErrorN-1
Phase Interpolator

FIG. 10G

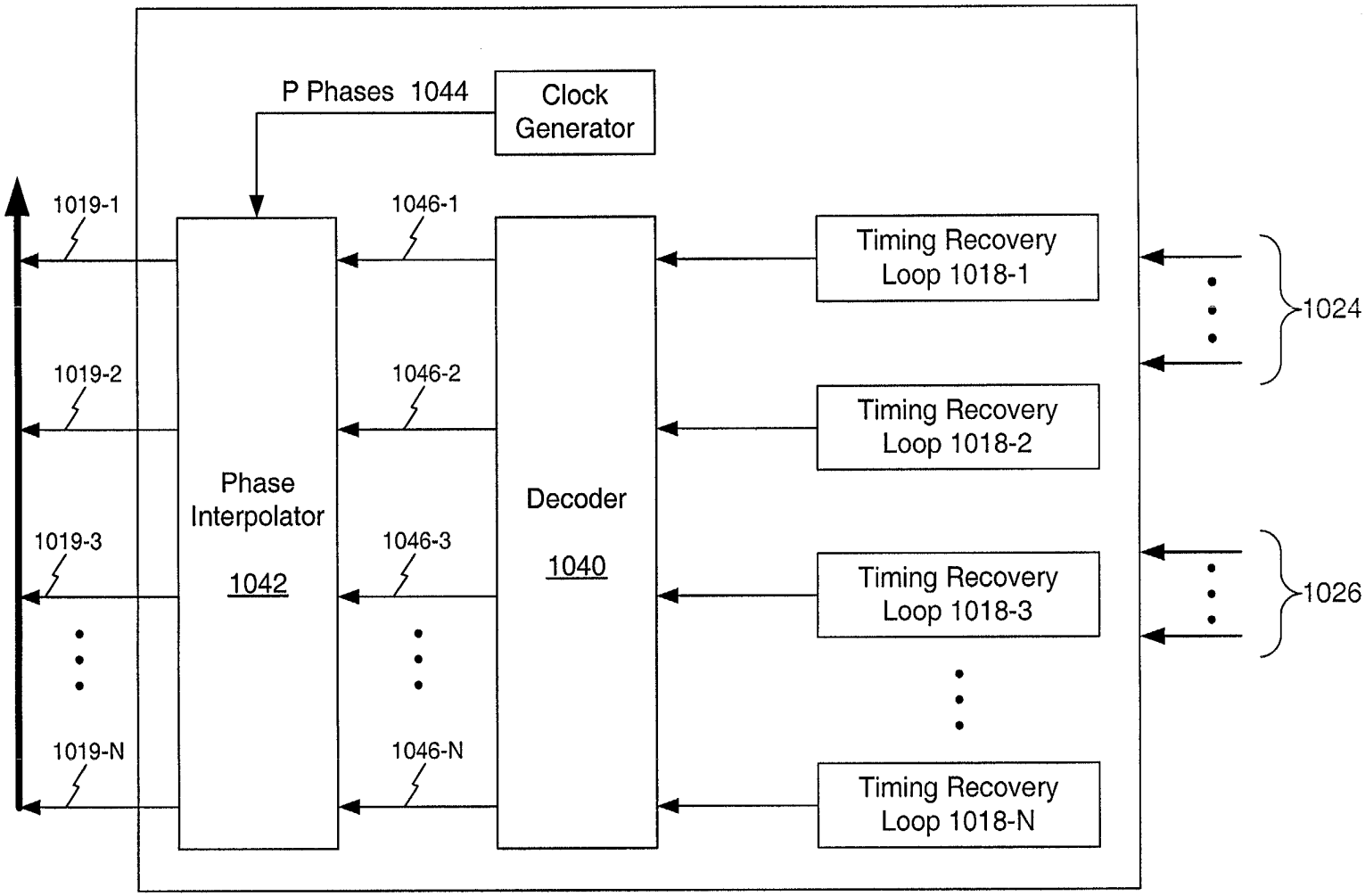

P Phases 1044
Clock Generator
1019-1
1046-1
1019-2
1046-2
1019-3
1046-3
1019-N
1046-N
Phase Interpolator
1042
Decoder
1040
Timing Recovery Loop 1018-1
Timing Recovery Loop 1018-2
Timing Recovery Loop 1018-3
Timing Recovery Loop 1018-N
1024
1026

FIG. 10H

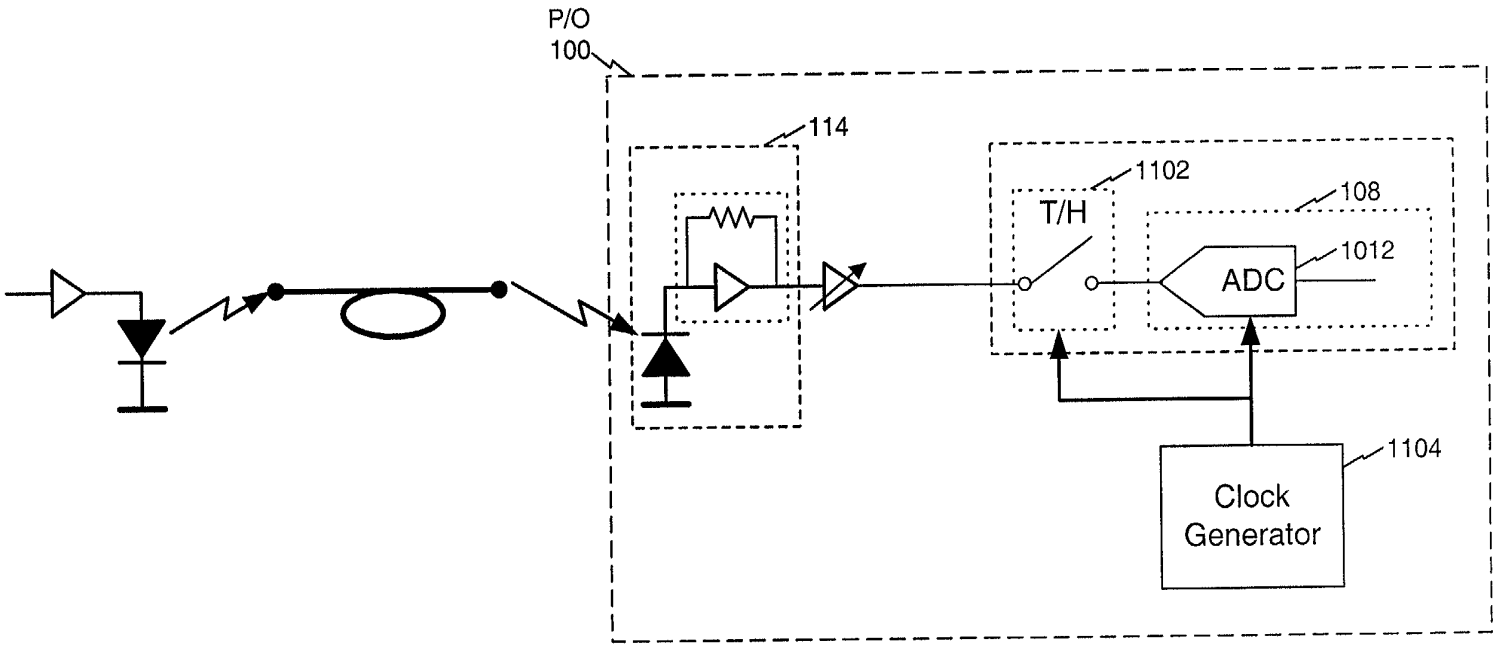


FIG. 11A

TOE270" 96860660

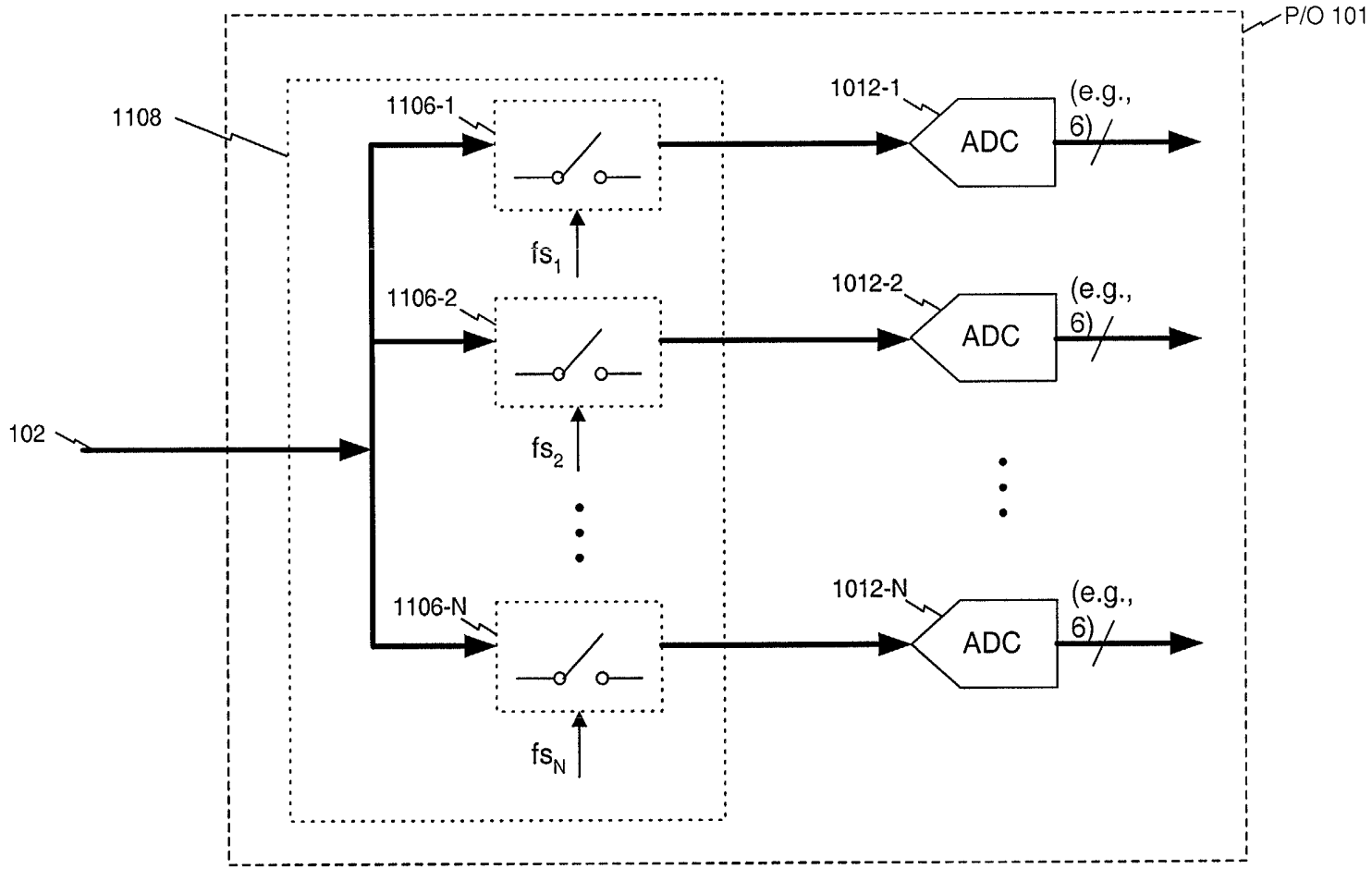


FIG. 11B

TDE2420 96960660

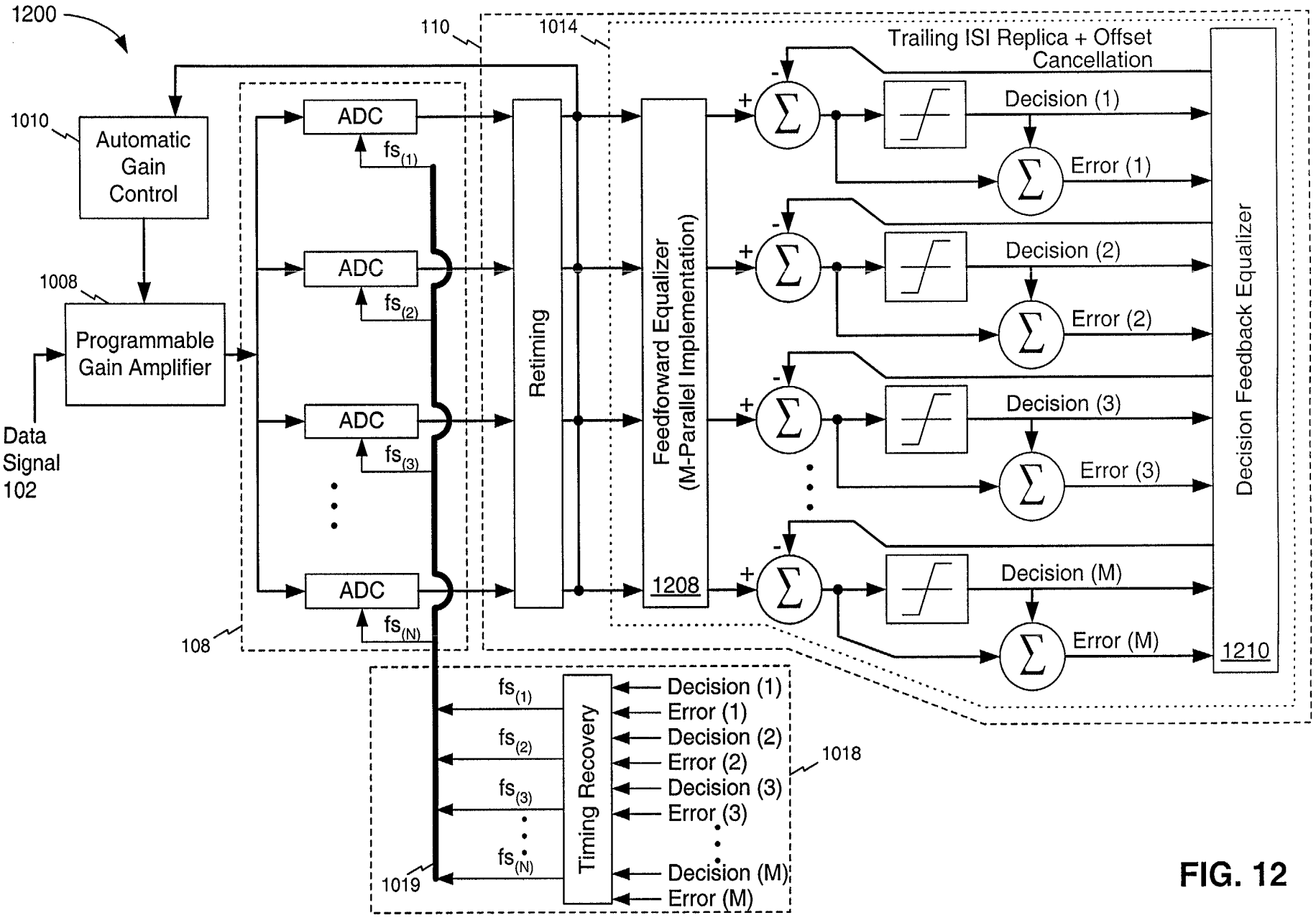
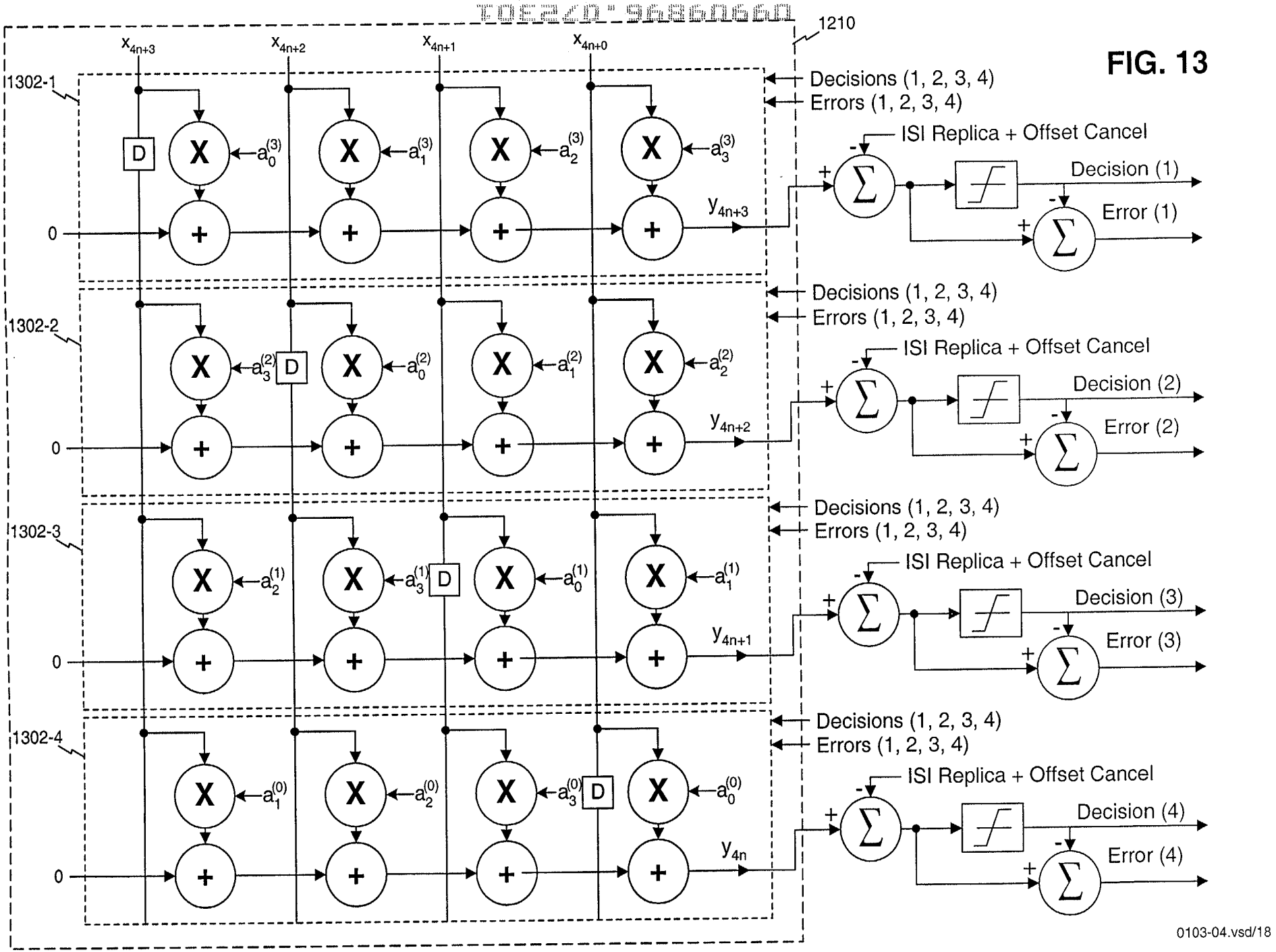


FIG. 12

0103-04.vsd/17

TOE2701 96360660

FIG. 13



TOS240 96860660

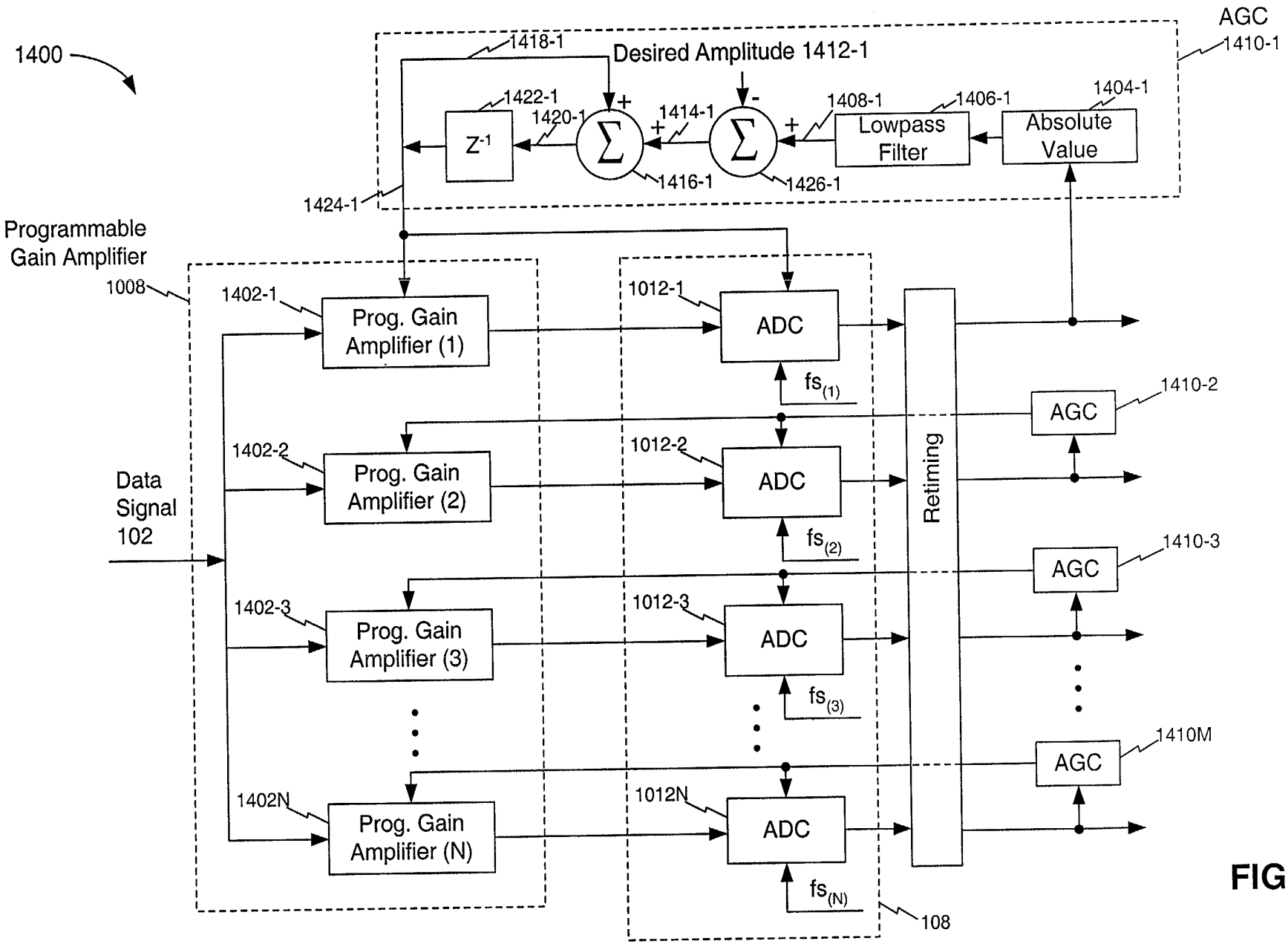


FIG. 14

0103-04.vsd/19

TOE220" 96960660

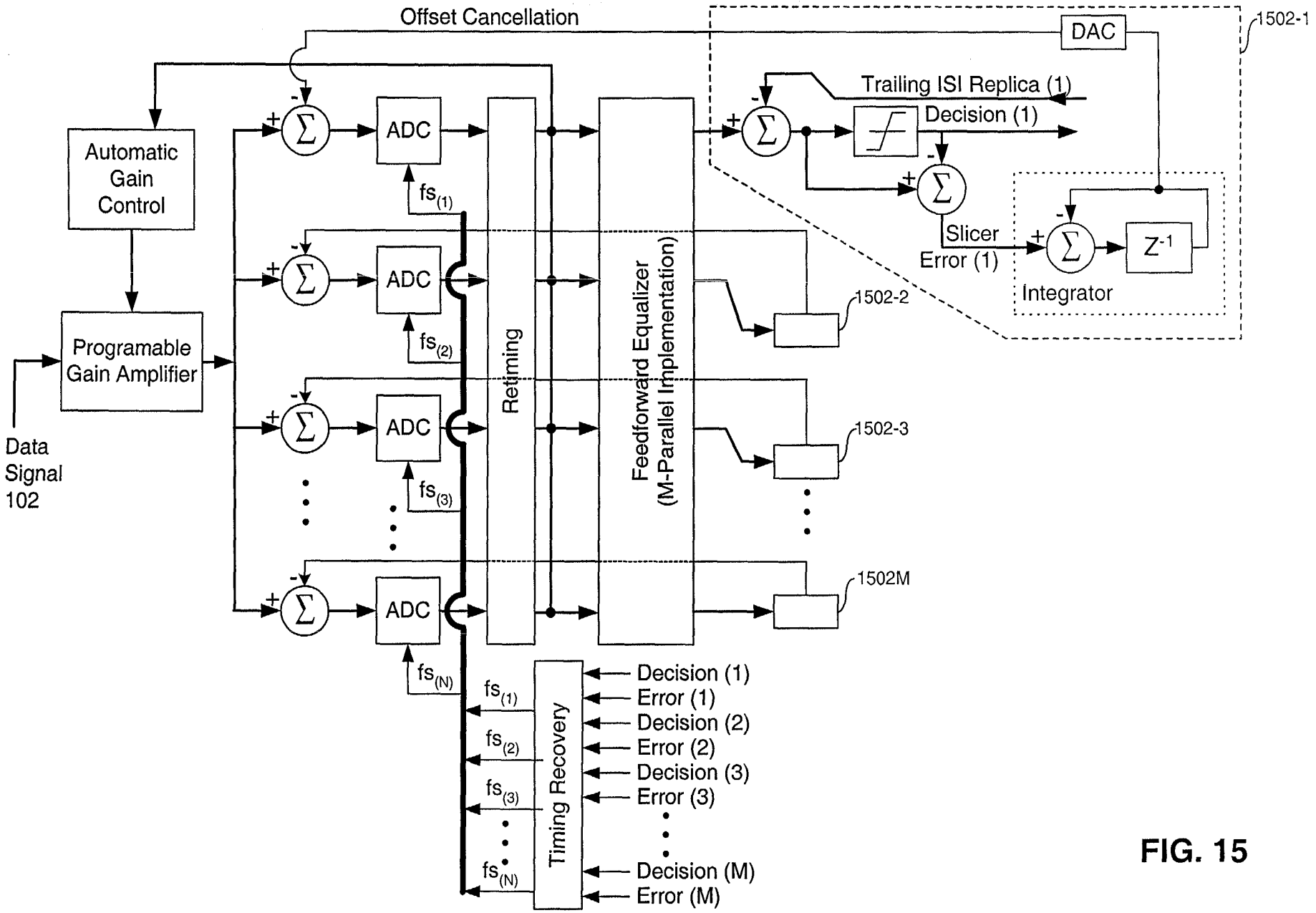


FIG. 15

0103-04.vsd/20

TOE240 "96860660

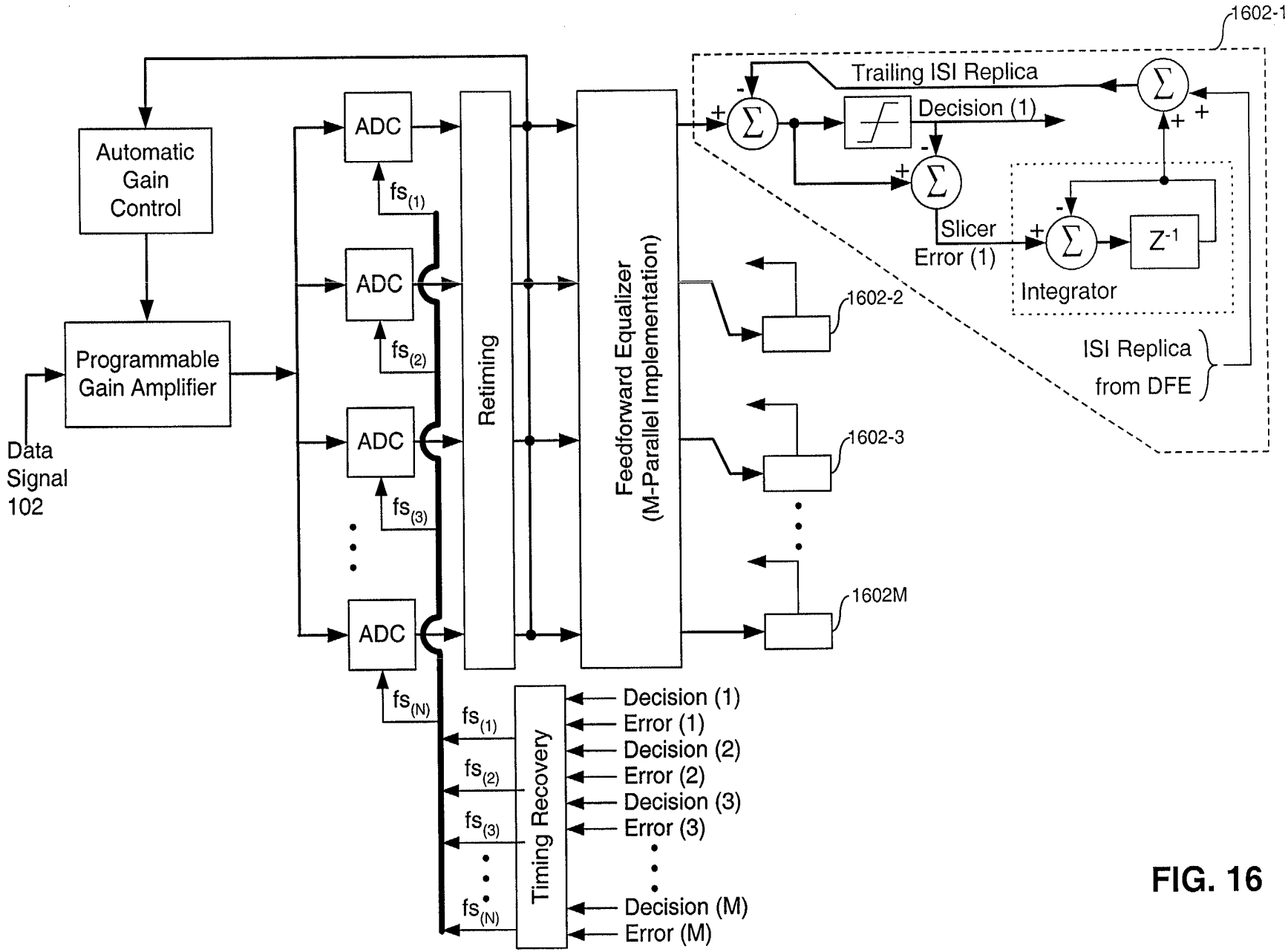


FIG. 16

0103-04.vsd/21

TOE220 96860660

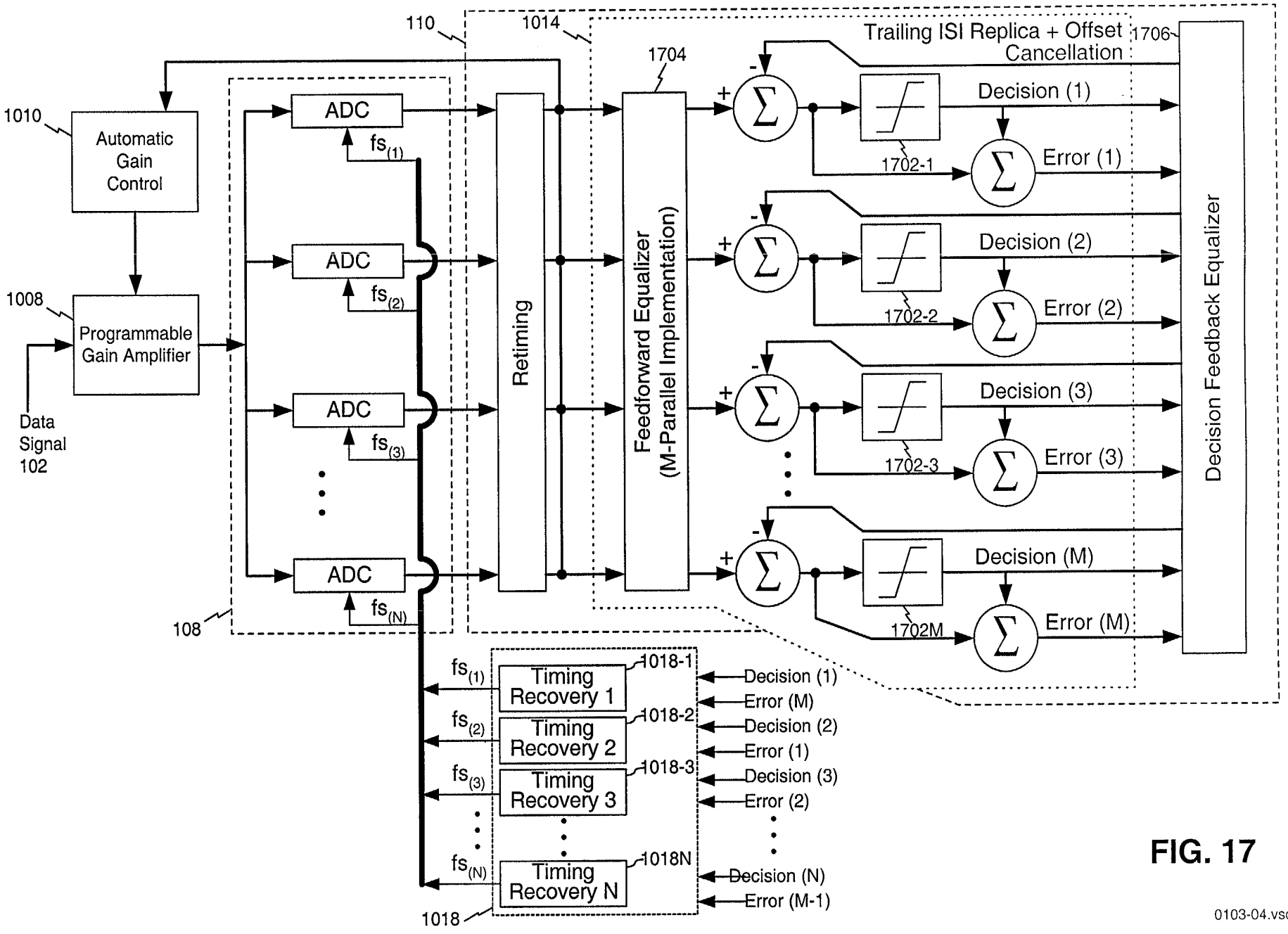


FIG. 17

0103-04.vsd/22

TOSZ20 96860660

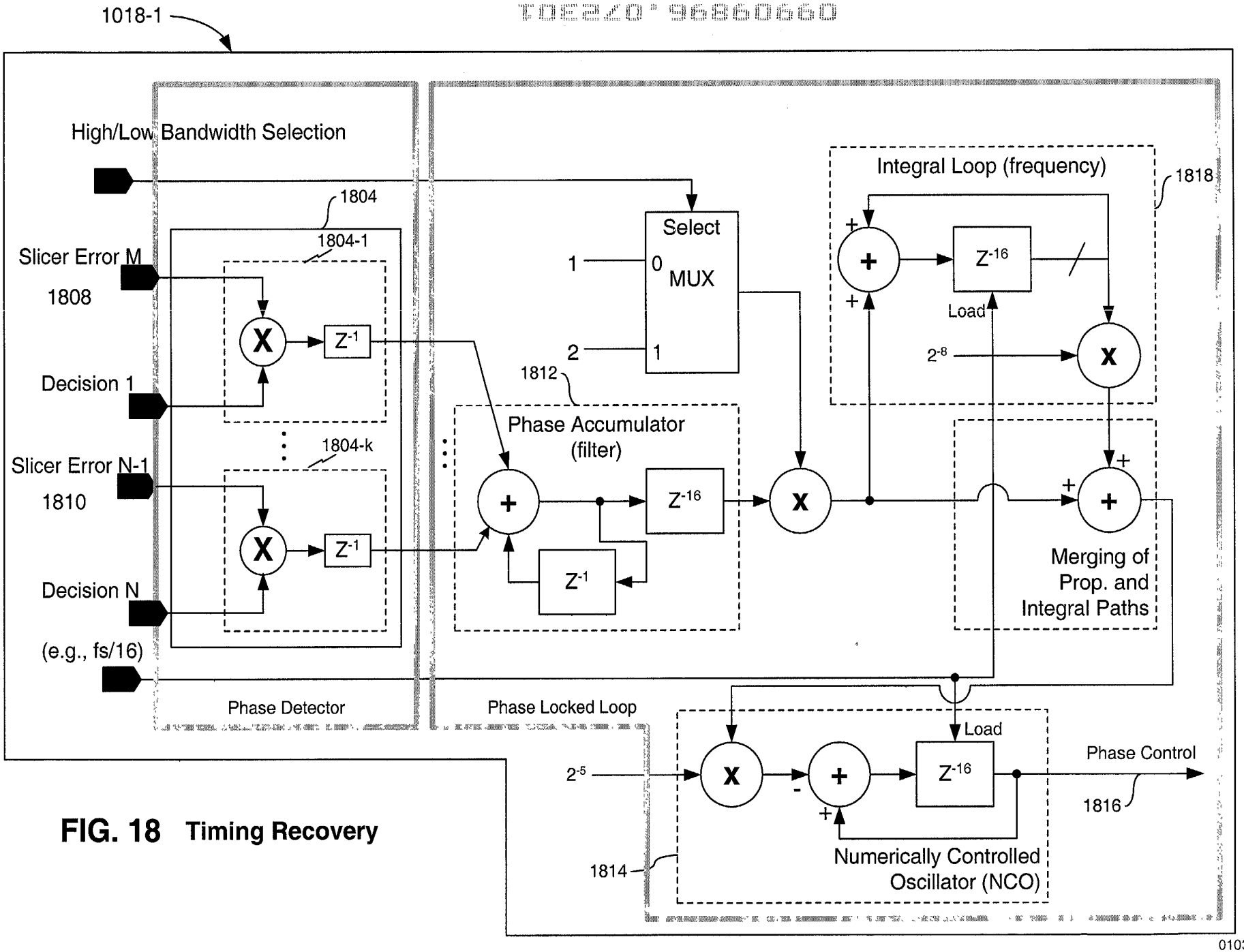


FIG. 18 **Timing Recovery**

0103-04.vsd/23

TOE2CD" 96860660

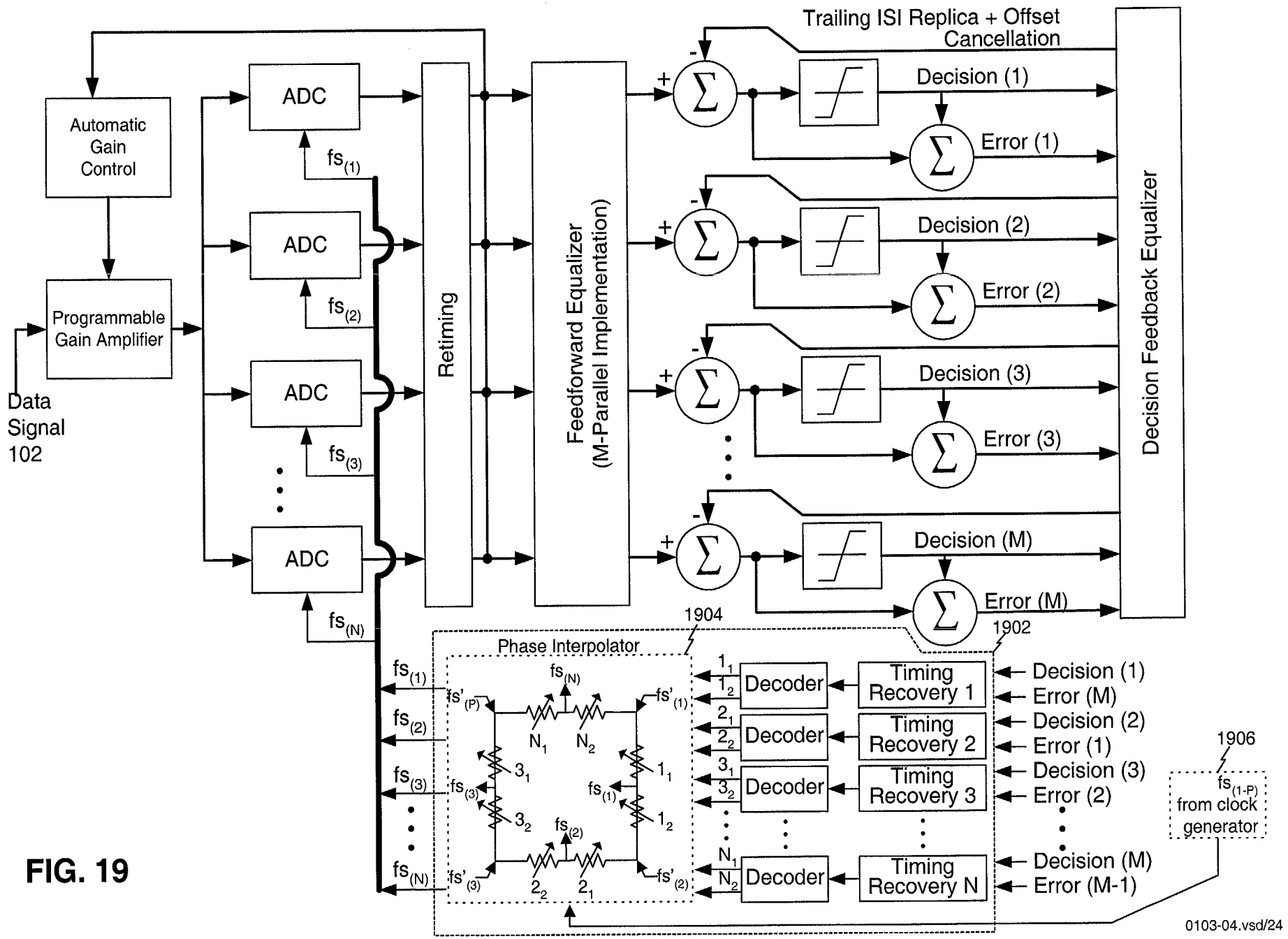
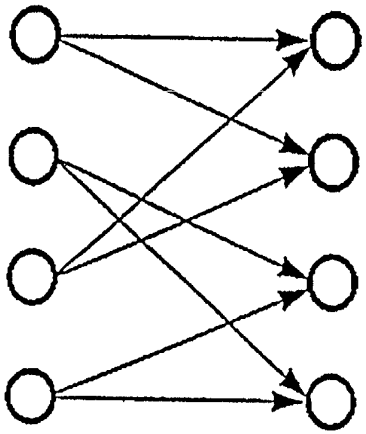


FIG. 19

TOE220" 96860660

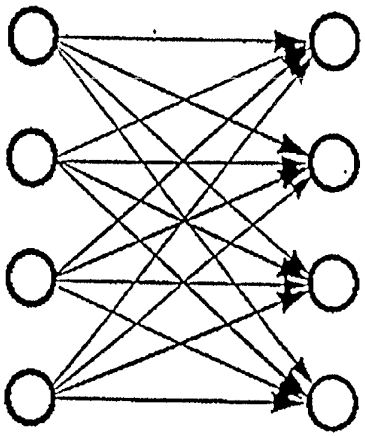
2000



4-state 1-step trellis (runs at a clock rate equal to the symbol rate)

FIG 20

2100



4-state M-step trellis (runs at a clock rate equal to $1/M^{th}$ of the symbol rate)

FIG 21

TOE270* 96860660

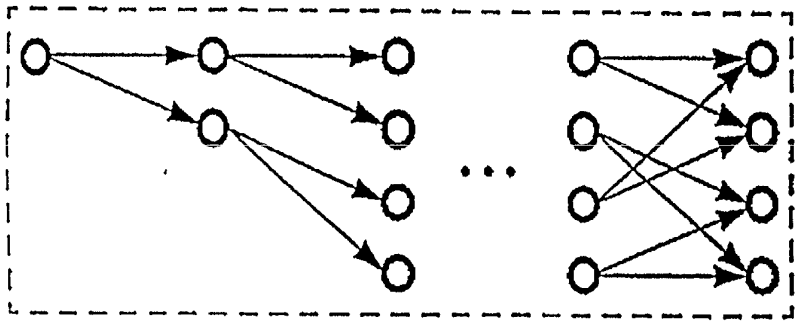


FIG 22A

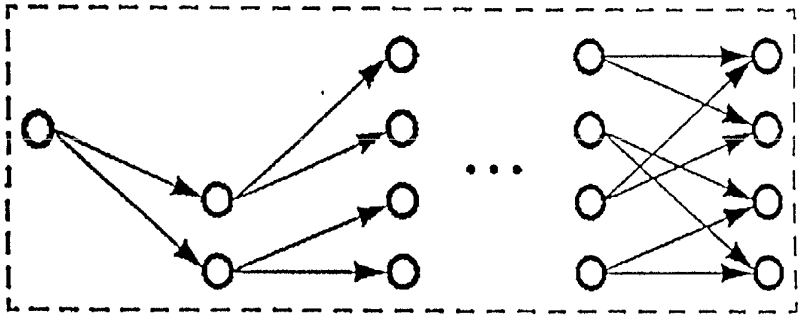


FIG 22B

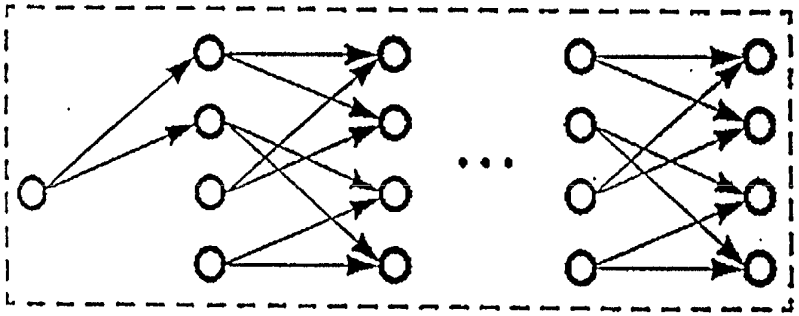


FIG 22C

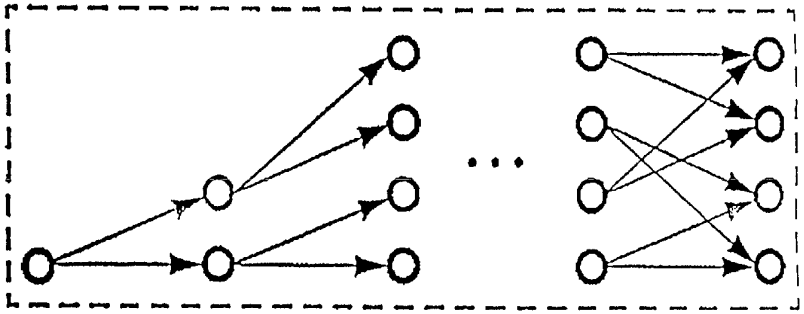
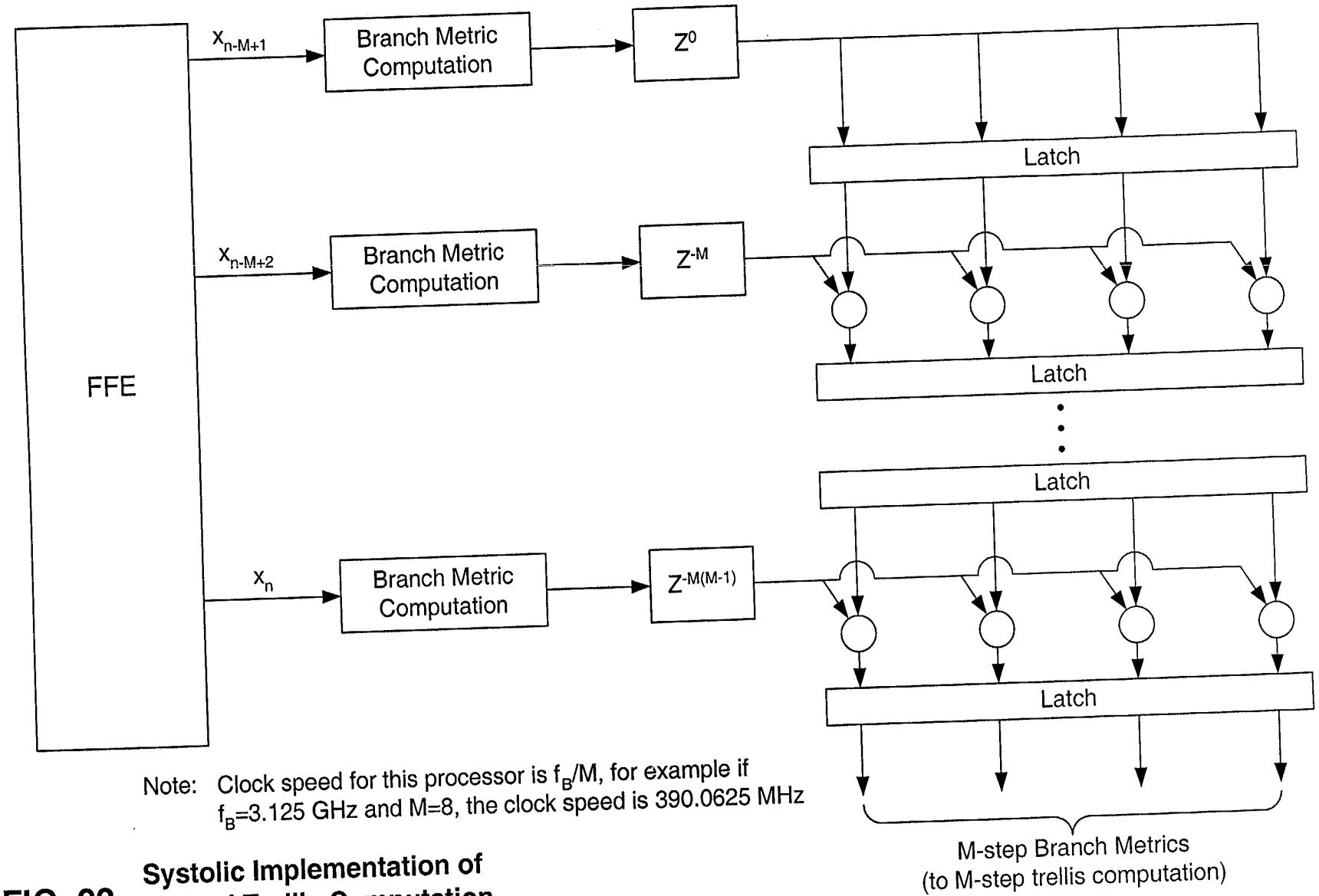


FIG 22D



Note: Clock speed for this processor is f_B/M, for example if f_B=3.125 GHz and M=8, the clock speed is 390.0625 MHz

FIG. 23 **Systolic Implementation of Rooted Trellis Computation**

0103-04.vsd/25

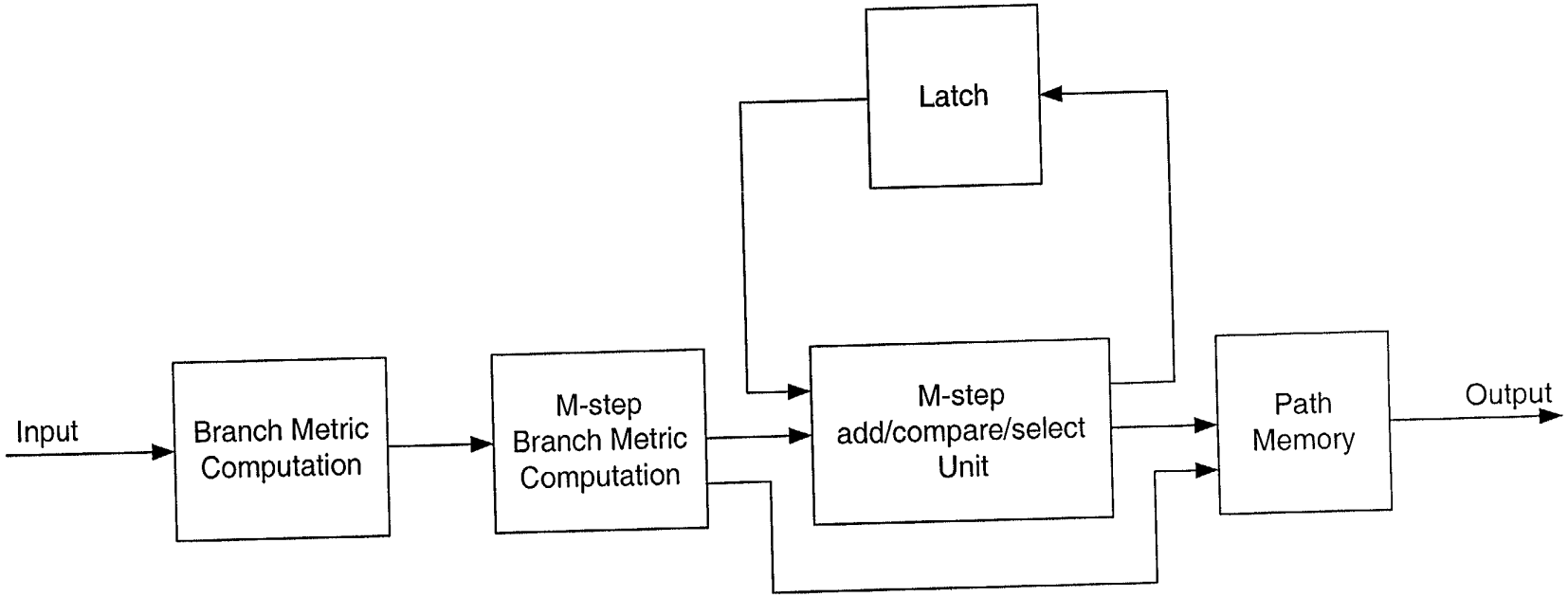


FIG. 24 Overall Block Diagram of Parallel Viterbi Processor